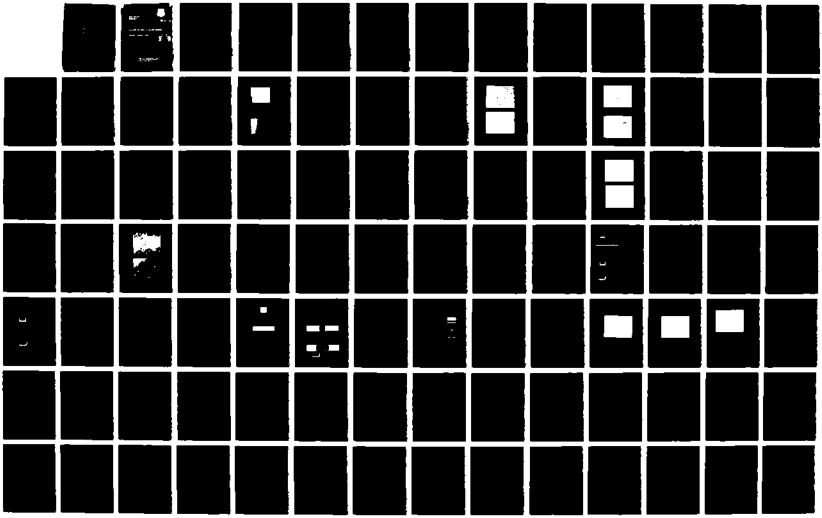
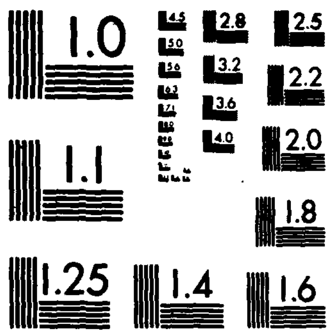
AD-A193 359 SILICON-ON-INSULATOR PIN DIODES(U) RENSSELAER POLYTECHNIC INST TROY NY DEPT OF ELECTRICAL COMPUTER AND SYSTEMS E NGINEERING E W MABY ET AL. DEC 87 1/2

UNCLASSIFIED RADC-TR-87-262 F19628-85-K-0038 F/G 9/1 NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

RADC-TR-87-262
Final Technical Report
December 1987

SILICON-ON-INSULATOR PIN DIODES

Rensselaer Polytechnic Institute

Edward W. Maby, Ronald J. Gutmann, Ted Letavic and Stephen Wu

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

This effort was funded totally by the Laboratory Directors' fund.

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, NY 13441-5700

A193 359

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b. RESTRICTIVE MARKINGS N/A
2a. SECURITY CLASSIFICATION AUTHORITY N/A 2b. DECLASSIFICATION / DOWNGRADING SCHEDULE N/A	3. DISTRIBUTION / AVAILABILITY OF REPORT Approved for public release; distribution unlimited.
4. PERFORMING ORGANIZATION REPORT NUMBER(S) N/A	5. MONITORING ORGANIZATION REPORT NUMBER(S) RADC-TR-87-262
6a. NAME OF PERFORMING ORGANIZATION Rensselaer Polytechnic Institute 6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION Rome Air Development Center (ESM)
6c. ADDRESS (City, State, and ZIP Code) Department of Electrical, Computer, and Systems Engineering Troy NY 12180	7b. ADDRESS (City, State, and ZIP Code) Hanscom AFB MA 01731-5000
8a. NAME OF FUNDING / SPONSORING ORGANIZATION Rome Air Development Center 8b. OFFICE SYMBOL (If applicable) ESM	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER F19628-85-K-0038
8c. ADDRESS (City, State, and ZIP Code) Hanscom AFB MA 01731-5000	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. 61101F PROJECT NO. LDFP TASK NO 10 WORK UNIT ACCESSION NO. C5

11. TITLE (Include Security Classification)
SILICON-ON-INSULATOR PIN DIODES

12. PERSONAL AUTHOR(S)
Edward W. Maby, Ronald J. Gutmann, Ted Letavic, Stephen Wu

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Final	FROM Mar 86 TO Jul 87	December 1987	110

16. SUPPLEMENTARY NOTATION
This effort was funded totally by the Laboratory Directors' Fund.

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Diode Phase Shifters
20	02		Silicon On Alumina
			Melt Recrystallization

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

~~This research program~~ is aimed toward a microwave monolithic integrated circuit (MMIC) technology using recrystallized silicon-on-insulator substrates. ~~Such a technology~~ would permit PIN diode phase shifters to be fabricated with higher power-handling capability and lower insertion loss than conventional MMIC control circuits using GaAs MESFETs. Moreover, at frequencies below 10 GHz, where substrate area requirements can be extensive, the silicon-on-insulator substrate technology can be less expensive. The research program stresses recrystallization of silicon-on-alumina films, followed by growth of silicon epitaxial layers and fabrication of surface-oriented PIN diodes.

In the second year of the program, we have accomplished the following:

(1) Recrystallization of silicon-on-alumina with various encapsulation and stress-relief layers, using both an electron-beam system and a graphite strip heater.

20. DISTRIBUTION / AVAILABILITY OF ABSTRACT ☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	21. ABSTRACT SECURITY CLASSIFICATION UNCLASSIFIED	
22a. NAME OF RESPONSIBLE INDIVIDUAL Alton F. Armington	22b. TELEPHONE (Include Area Code) (617) 377-5017	22c. OFFICE SYMBOL RADC (ESM)

DD Form 1473, JUN 86 Previous editions are obsolete.

SECURITY CLASSIFICATION OF THIS PAGE
UNCLASSIFIED

(2) Evaluation of the effect of stress on film quality, which indicates directions for improved device-quality films;

(3) Design and initial fabrication of surface-oriented PIN diodes on single crystal silicon to demonstrate device design concept;

(4) Evaluation of future directions for the research program.

This report covers the second-year results. Particularly noteworthy is the first recrystallization of silicon-on-alumina films and the first fabrication of surface-oriented PIN diodes with doped polysilicon handles for P+ and N+ injecting contacts.

ACKNOWLEDGEMENTS

The principal investigators acknowledge the capable assistance of Mr. Ted Letavic in executing many of the tasks of this program, particularly the extensive electron-beam system modifications, recrystallization studies and thin-film stress analysis and Mr. Stephen Wu in the device design and processing development. The assistance provided by Dr. Carl Thompson and Mr. Jim Im in using the strip heater recrystallization facility at MIT is gratefully acknowledged. The use of the processing facilities at the Rensselaer Center for Integrated Electronics and the assistance of Mr. Daniel Pulver were critical to the PIN diode fabrication. Mr. John Ayers performed the x-ray diffractometer experiments useful in our film evaluation. The encouragement and support of the contract monitors, Dr. Eurig Davies and Mr. Alton Armington, have been very helpful to the success of the program.

Edward W. Maby

Ronald J. Gutmann

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

Monolithic microwave integrated circuits (MMICs) containing transceiver (transmitter/receiver) circuitry have not been incorporated into microwave systems principally because of either inferior performance and/or excessive cost. The high costs result from an expensive technology base (usually epitaxial GaAs channels on semi-insulating substrates or ion-implanted channels), inadequate use of wafer area (due to the large-area requirements of the passive circuitry) and the relatively small number of transceivers needed in microwave systems compared to digital applications (even with planar phased arrays). Si PIN diodes have significantly enhanced RF performance compared to GaAs MESFETs for control applications like phase shifting, since both switching figure-of-merit and power-handling capability are increased. However, production reproducibility, performance advantages due to lower parasitics and lower cost potential drive innovative research in MMICs for this, and other, microwave applications.

Most of the research in MMICs involves either GaAs epitaxial layers for highest performance or ion-implanted layers for lower cost on semi-insulating GaAs. The technology suffers from yield problems, since large areas of device-quality layers are mandatory. In most technologies to date, GaAs metal-semiconductor (or Shottky-gate) field-effect transistors (MESFETs) are the active device building blocks. These versatile devices have been used not only in traditional transistor applications such as low-noise and power amplifiers, but also in frequency conversion (e.g. mixer) and control (e.g. switches and phase shifters) components. Performance as a control device is particularly poor compared to Si PIN diodes because of the relatively large on-resistance (~2 to 6 ohms) inherent with the device structure and the limited RF voltage capability (~20 to 30 volts drain-to-source). The high resistance results in appreciable dissipation in the device and reduced average-power handling capability, while the reduced voltage handling results in low peak-power performance. Recent results indicate that GaAs PIN diodes may become viable control devices, with applications in MMIC technology. However, the relatively low lifetime (10 to 100 nanoseconds for lightly-doped high-quality GaAs) of this direct-band-gap material forces thin I-layer dimensions and relatively low peak-power capability compared to Si PINs.

While GaAs MMICs are being established as a viable technology, the production cost of such a technology remains a serious concern. In this program, silicon-on-insulator (SOI) technology is investigated as a potential alternative offering the promise of lower cost as well as improved control-component performance. Conceptually, a silicon film is deposited over a microwave-quality dielectric substrate and recrystallized, serving as a base for further processing. Such a silicon-on-insulator technique would result in a monolithic microwave technology which is:

1) compatible with highest control-device figure-of-merit and highest control device power handling, namely the Si PIN diode.

2) potentially a much lower cost technology than GaAs MMICs.

3) compatible with high-power system requirements below 10 GHz.

4) potentially extendable to other semiconductors (including compound semiconductors), perhaps on the same substrate.

The two-year research program has been concerned with the initial evaluation of the feasibility of a silicon-on-insulator MMIC technology. In particular, the program has focused on PIN diodes for a 40-watt, 5.3-GHz, low-loss monolithic phase shifter as a test vehicle. While fabrication of a complete phase shifter is beyond the scope of the research program, we delineated key problems affecting the technology and evaluated the potential for future microwave systems. PIN diodes are particularly difficult for a silicon-on-insulator technology since a reasonable high-injection-level recombination lifetime is needed to obtain conductivity modulation under forward bias. However, they are critically important in transceiver modules for phased arrays and therefore an excellent test vehicle for evaluating the potential of a silicon-on-insulator technology for MMICs.

At present, a monolithic 40-watt peak power, 4-watt average power, 5.3-GHz, low-loss phase shifter cannot be realized in either GaAs or Si. In GaAs, the large on-resistance of MESFETs results in high loss and low average-power handling capability. In addition, the peak-power handling capability is limited by drain-to-source breakdown to less than 10 watts. GaAs PINs have minority carrier lifetimes which are too low, resulting in thin I layers and low peak-power handling capability. While the phase-shifter requirements are well within the capability of Si PIN diodes, the lack of semi-insulating silicon substrates with sufficient dielectric quality is incompatible with conventional semiconductor monolithic implementation. More specifically, the dielectric loss of a silicon MMIC transmission line prohibits high-performance circuits.

The actual PIN diode requirements depend not only on the phase-shifter component specifications (5.3 GHz, 40 watts peak, 4 watts average, 0.5 microseconds switching time) but also on the phase-shifter circuit design. However, the PIN diode/phase shifter circuit designs are mutually coupled by the material/device performance capabilities. To guide the material/device research program for a silicon-on-insulator technology, we conservatively assumed that the PIN diode must handle twice the RF line voltage under reverse bias and twice the RF line current under forward bias. That is, we assume that the PIN diode is capable of performing as a single-pole-single-throw switch. Assuming a 50-ohm transmission line and conservative silicon PIN diode design rules, we arrived at a 3-mil-diameter diode with a 12-μm I-layer thickness for a conventional vertical diode configuration. Additional aspects of the PIN diode design, a comparison of lateral and vertical configurations and our best estimate of performance capability is discussed in detail in the First Annual Report [1].

A suitable substrate for MMIC applications must have a low-loss tangent dielectric with large thermal conductivity and a coefficient of expansion closely matched to silicon, and it must be available at reasonable cost. The silicon film over the substrate must be free from macroscopic defects and possess long carrier lifetime. Both cost and lifetime factors preclude the choice of silicon-on-sapphire, the only thin-film SOI system which can be produced by heteroepitaxial growth. To date, most other SOI technologies have produced thin silicon films over an oxidized silicon substrate by means of a solid- or liquid-phase recrystallization process. However, for the MMIC application, the underlying silicon layer would provide undesired dielectric loss and negate the advantage of recrystallized film processing.

A substrate which meets many MMIC requirements is alumina, as it is already used as a substrate in hybrid MICs and, in single-crystal form (i.e., sapphire), as a substrate for silicon field-effect devices. Recent work has shown that polycrystalline silicon films can be recrystallized over a sapphire substrate by a liquid-phase process, and the electrical characteristics of these films are similar to those for conventional heteroepitaxial silicon-on-sapphire. A similar recrystallization process for polycrystalline silicon deposited over alumina should produce improved results since the thermal expansion of alumina can be better matched to that of silicon.

Thus, this research program emphasizes recrystallization of silicon-on-alumina, with evaluation of the suitability of these films for subsequent PIN diode fabrication and MMIC implementation. The remainder of the report covers:

- silicon-on-alumina recrystallization considerations
- silicon-on-alumina recrystallization results
- surface-oriented silicon PIN diode design and fabrication
- evaluation of status and future directions

For continuity and program evaluation considerations, the Abstract, Table of Contents and Plans for the Second Year (from the First Annual Report) are included in Appendix A.

2. SILICON-ON-ALUMINA RECRYSTALLIZATION CONSIDERATIONS

In this section, we present an overview of recrystallization research which serves as a foundation for our technical approach (Section 2.1), followed by a discussion of the factors influencing the encapsulation layer prior to the actual recrystallization process (Section 2.2). Then we describe the impact of a non-silicon substrate on zone-melt recrystallization (ZMR) of silicon (Section 2.3), the key section in Chapter 2. This section is divided into a number of subsections which describe factors in controlling the effectiveness of ZMR on alumina substrates.

2.1 Technical Background

Liquid-phase processes for the realization of single-crystal silicon films over various insulating substrates all require the movement of a molten silicon zone over the substrate surface. The processes differ mainly by the shape of the molten zone and the type of heat source which is used. First experiments used a focused laser beam to produce a molten spot with circular symmetry[2], and later recrystallization results were improved by judiciously shaping the spot.[3] Other experiments have used a resistively-heated graphite strip[4,5] or an electron beam[6,7] to produce a molten line.

Apart from the results of various crystallogr phic diagnostic procedures, one measure of the success of a recrystallization experiment is the channel carrier mobility and sub-threshold leakage current of insulated-gate field-effect transistors fabricated on the recrystallized film. For the case of oxidized silicon substrates, line-source experiments have produced the best, and most consistent, device results thus far.[4,8,9]

Typical recrystallization results for the case of 0.5-µm-thick silicon films and a graphite-strip source are shown in Fig. 2.1.[5] As indicated by the orientation pattern of a matrix of anisotropically etched square pits (pit grid), the recrystallized silicon films consist of large (2 mm x 1 cm) grains which are seeded from a transition region at the edge of the film and separated by large-angle grain boundaries. Within the large grains, at approximate 25-μm intervals, are line defects which are generally parallel to one another and to the scan direction of the graphite strip. These parallel line defects are surface intersections of planar defects that cut the entire film thickness more or less perpendicularly; they are believed to be associated with angular deviations of the order of one degree or less, so they are called subboundaries.[5] The films have nearly uniform (100) crystallographic texture.

Experiments have shown that majority-carrier transport is impeded by large-angle grain boundaries which transversely cross resistor bars fabricated in recrystallized silicon films, and the turn-on characteristics of similarly oriented field-effect transistors are also influenced.[10] Enhanced diffusion of impurities along large-angle grain boundaries can also merge the source and drain regions of parallel-oriented field-effect transistors.[11] Fortunately, the density of large-angle grain boundaries can be reduced by double-pass recrystallization or substrate seeding.[12] Subboundaries have relatively little influence on majority-carrier bulk transport or the turn-on characteristics of field-effect transistors, and the degree of lateral diffusion along subboundaries is much less than that for large-angle grain boundaries. Subboundaries must be avoided, however, when minority-carrier lifetime is important.[13] Although it is difficult to completely eliminate subboundaries from thin line-source-recrystallized films, special procedures can be employed to confine the subboundaries to specific positions so that devices can be fabricated in between them.[14]

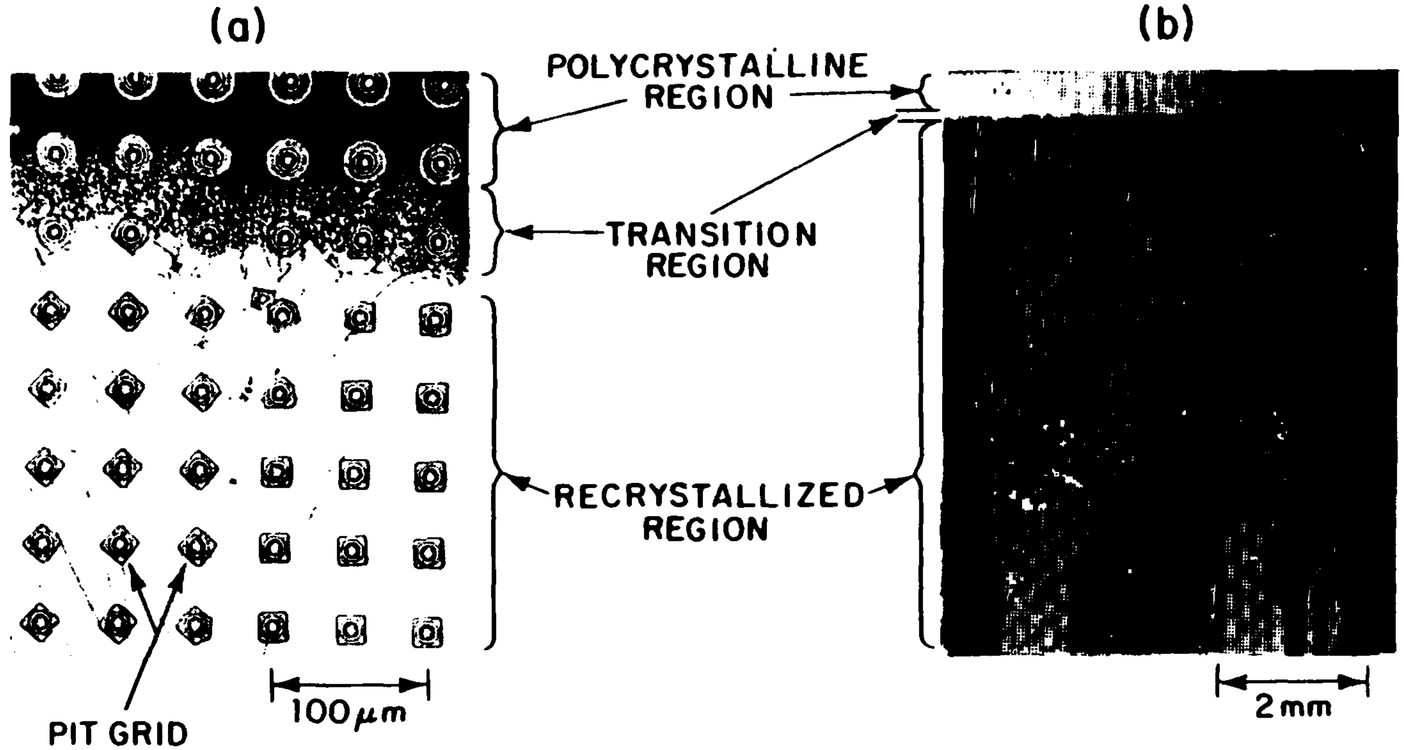


Figure 2.1: Typical line-source recrystallized films (see text)

There have been a limited number of line-source recrystallization experiments which concern silicon over sapphire and fused quartz.[15,16] For the case of sapphire substrates, the recrystallized silicon film is under compressive stress at room temperature; whereas, for the case of fused-quartz substrates, the recrystallized silicon film is under tensile stress, and care must be taken to avoid the formation of cracks in the film.

The silicon-on-sapphire line-source recrystallization results suggest that high-quality silicon-on-alumina films for the fabrication of PIN diodes can be produced by a similar procedure. For our experimental program, we chose to principally use a rapidly scanned electron beam in order to approximate a line source since we believed that this would be superior to a graphite-strip or an arc-lamp source in terms of control of the molten zone. The electron-beam system required considerable development (see first annual report), so we also employed a graphite-strip recrystallization apparatus during the course of our program to obtain initial results which were used as a comparative aid.

2.2 Factors Influencing Encapsulation Layer

Line-source recrystallization experiments have all employed some form of encapsulation layer over the silicon film in order to induce recrystallized film texture and promote wetting of the substrate beneath the film. For the case of oxidized silicon substrates, the film texture is made more uniform as the thickness of a chemical-vapor-deposited (CVD) silicon dioxide encapsulation layer is increased,[17] but the improvement is marginal for thicknesses greater than about 2 μm. Studies have shown that the agglomeration problem tends to be avoided if nitrogen is present at the interface between the silicon film and the encapsulation layer prior to recrystallization.[18] This has been achieved by sputtering silicon nitride over the silicon dioxide encapsulation layer and by depositing the silicon dioxide with a plasma CVD process which uses N_2O as a source gas.[19] The specifics of encapsulation-layer preparation remain less of a science than an art.

The stresses on the encapsulation layer are reduced as the width of the molten zone is decreased. The electron-beam line source can yield a more narrow molten zone than that which is produced by a graphite strip or arc lamp, so the electron-beam recrystallization experiments may be relatively forgiving in terms of the agglomeration problem.

By tradition, most silicon-on-insulator recrystallization experiments have used 0.5-μm-thick silicon films. Thicker films lead to increased subboundary spacing,[17] and significant reduction in defect density is observed in thick films when the encapsulation layer is patterned to provide vent openings for excess oxygen which is dissolved in the molten silicon.[20]

These factors, abstracted from the literature and our own experiments on silicon-on-oxidized silicon have provided a useful guide for this program. However, the impact of a non-silicon substrate was determined to have great significance as described in Section 2.3 below.

2.3 Impact of Non-Silicon Substrate on ZMR of Silicon

2.3.1 Sample Preparation

Silicon-on-insulator (SOI) samples are fabricated by chemical vapor deposition of various thin films onto a suitable substrate. To a large degree, the quality of the deposited films is dependent upon the surface characteristics of the substrate material. For zone melt recrystallization (ZMR), it is desirable to have optically flat, uniform surface films. Surface analysis of commercial grade alumina substrate material indicates that the surface morphology resembles that of a polycrystalline composite, with a defect structure dominated by grain voids.

Fig. 2.2A is a SEM micrograph of commercial-grade alumina. It is evident that the grain voids are oriented in such a manner as to form overhangs which trap gaseous species during atmospheric pressure depositions. Expansion of entrapped gaseous species upon heating results in destruction of the surface films, so gas entrapment must be avoided. The surface structure of commercial-grade alumina can be altered by planarization techniques such as enhanced mechanical polishing and phosphosilicate glass (PSG) reflow. Enhanced mechanical polishing of the substrate is performed at high pressure with a diamond slurry, while PSG reflow constitutes viscous flow of a phosphorous-rich silicon dioxide film at high temperature. Fig. 2.2B illustrates the surface characteristics of commercial-grade alumina which has been planarized by PSG reflow at 1000°C. The surface is optically flat, but gas entrapment still cannot be completely avoided due to the finite viscosity of the PSG film.

Fig. 2.3 is a SEM micrograph of an ultra-grade alumina substrate which has been planarized via enhanced mechanical polishing. A 1.5-μm-thick layer of CVD silicon dioxide has been deposited onto the surface to increase resolution. The surface is characterized by large optically flat mesas which are

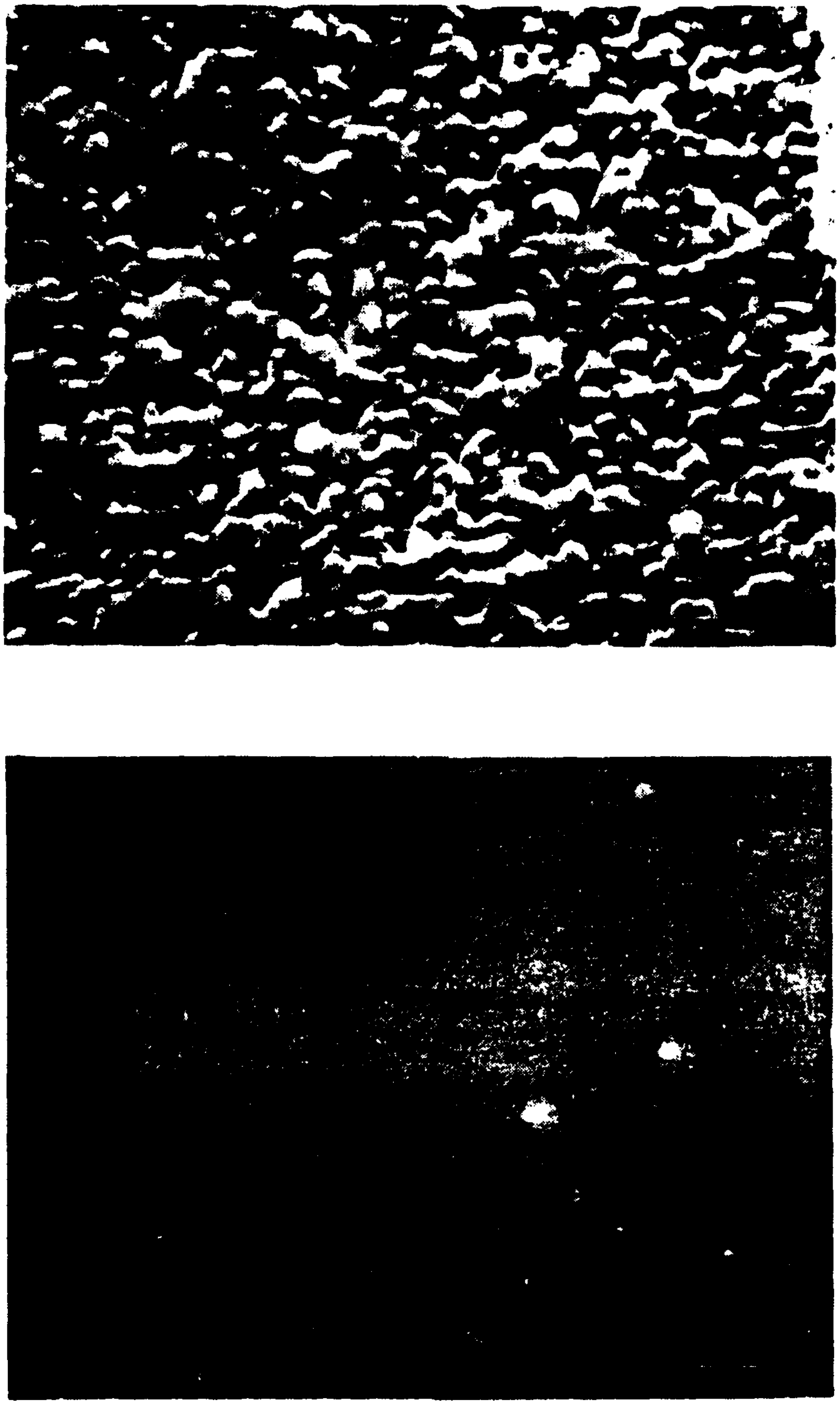


Figure 2.2: Comparison of Commercial Grade Substrate Alumina at 5Kx Magnification (A) As Received and (B) with PSG Reflow Coating

impacted by grain pullouts and polishing scoring lines. The surface finish of ultra-grade alumina, as measured by the mean deviation from a center line, is ±100A. Ultra-grade material was selected for all silicon-on-alumina fabrication since the PSG reflow technique does not completely alleviate gas entrapment. Moreover, the overhang areas in the PSG-planarized commercial-grade alumina result in local stress concentrations which increases the probability of critical crack tip formation. Thus, ultra-grade alumina is mechanically stronger than commercial-grade material, so it is less susceptible to thermally related mechanical failure.

2.3.2 Energy Absorption Considerations

During the zone-melt recrystallization process, the sample to be recrystallized is heated to a uniform substrate bias temperature prior to application of the primary heat source. In our present electron beam system, the substrate bias temperature is achieved by radiant heating from an arc lamp assembly (with blackbody radiation centered at 0.84 μm), and the primary heat source is a focused, raster-scanned electron beam. It has been experimentally observed that the surface temperature attainable with arc-lamp heating of alumina substrates is considerably less than that with silicon substrates. The substrate bias temperature is a crucial process parameter, so the energy absorption characteristics of alumina have been explored in detail.

The maximum surface temperature attainable on a silicon substrate (when the arc lamps are driven at the maximum power which is compatible with the vacuum system design) exceeds that of alumina substrates by approximately $150^{o}C$. Fig. 2.4 is a plot of surface temperature versus DC arc-lamp current for several different material structures. It is desirable to heat alumina substrates to at least $1000^{o}C$ prior to the application of the primary heat source in order to avoid thermal shock failure of the substrate and thermal

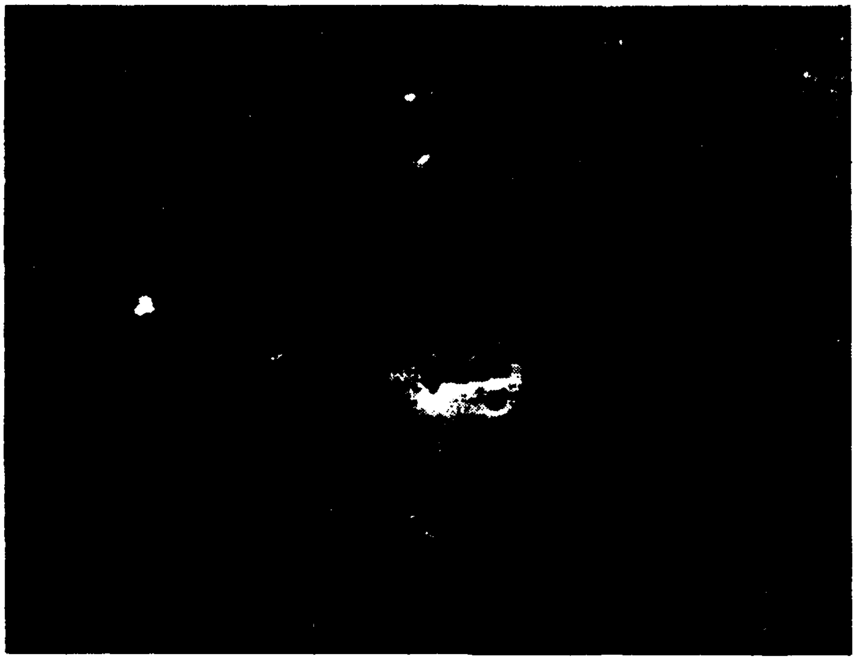


Figure 2.3A: Ultra Grade Substrate Alumina, SEM 40^{o} 5Kx
(Polish by Valley Design)

Figure 2.3B: Ultra Grade Substrate Alumina, SEM 40^{o} 10Kx
(Polish by Valley Design)

spalling of the surface films. In order to design a silicon-on-alumina materials structure which can be heated to 1000°C with the radiant arc lamps, the energy absorption and heat transfer characteristics of alumina SOI structures must be considered.

The maximum surface temperature attainable by a composite material is a function of various thermophysical properties such as spectral absorption, thermal conductivity and emissivity. An energy-balance equation can be formulated which incorporates the dominant modes of heat transfer and energy absorption, and it can be solved for the surface temperature.

To quantify the dominant mode of energy absorption for alumina, its band structure must be considered. Alumina is a ceramic insulating material with a band gap in excess of 4 eV. Thus, direct band-to-band absorption is forbidden at any bias temperature. The dominant mode of energy absorption in bulk alumina is impurity dominated, so the absorption characteristics are a function of impurity content. This has been verified experimentally; alumina samples with low chemical purity absorb a greater fraction of the incident spectrum. Radiant energy which is not absorbed by the alumina substrate is incident upon the various surface films from below. The polysilicon layer appears as a free-electron metal at temperatures in excess of 300°C, but it does not absorb appreciable radiation because it is extremely thin. The radiation transmitted through the polysilicon will not be absorbed by the surface silicon dioxide layers, so the dominant mode of heat transfer in thin-film-on-alumina structures is absorption in the bulk alumina and subsequent conductive heating of the surface films.

The energy absorption mechanism in silicon substrates contrasts drastically with that of the alumina system. Silicon is a semiconductor at low temperatures where it exhibits band-to-band absorption. At temperatures in ex-

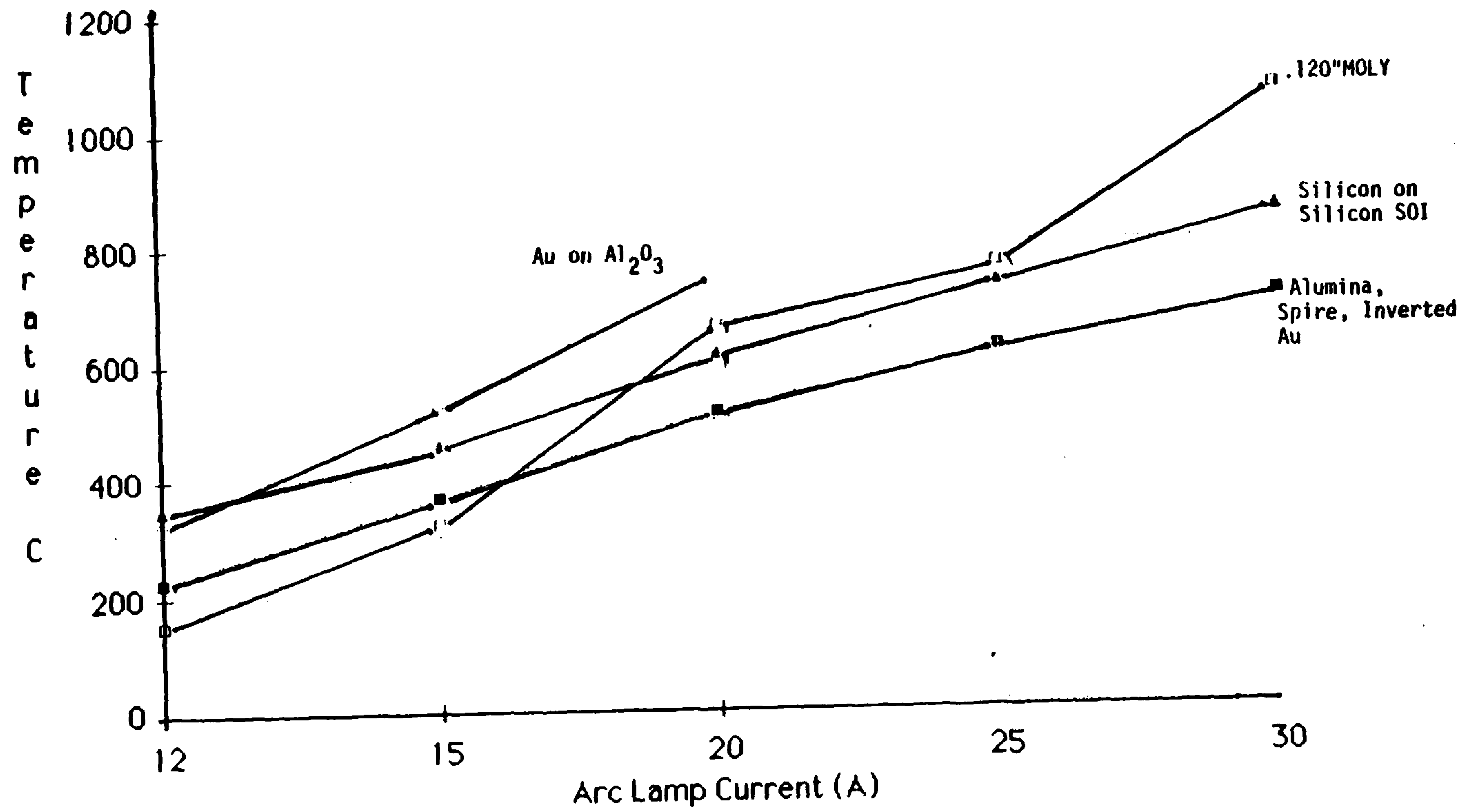


Figure 2.4: Substrate Temperature Dependence Upon Arc Lamp Current for Various Materials

cess of 300°C, the substrate silicon resembles a free-electron metal, so the primary absorption mechanism is via free-carrier processes. As with the alumina substrate, radiant energy absorbed in the bulk is conducted to the surface films, but a greater fraction is absorbed by the substrate.

Energy transfer mechanisms from the sample surface must also be quantified. Within the electron-beam system, the resistance to conductive heat transfer to the surroundings is much greater than the resistance to radiative heat transfer, so the surface temperature is controlled by the efficiency of surface radiant heat transfer. Lumped thermal models of silicon-on-alumina and silicon-on-oxidized silicon structures in a vacuum are characterized by a Biot number of about 10^{-4}. This indicates that temperature gradients are very small in the substrates and that the surface temperature is primarily a function of the surface-film emissivity coefficient and the surrounding environment temperature.

Since radiant heat transfer from the sample surface is primarily a function of the surface emissivity, it can be discerned that the anomaly in surface temperature between structures which feature silicon and alumina substrates cannot be attributed to surface effects. Thus, energy absorption in the bulk is responsible for the differen'e in surface temperature.

The energy absorption of alumina can be altered by shifting the incident spectrum towards the ultraviolet to decrease transmittance, or by depositing an infrared absorber onto the alumina substrate to absorb the incident radiation and heat the alumina conductively. The extremely low Biot number (10^{-4}) associated with the lumped thermal model for silicon-on-alumina indicates that this latter approach is feasible if a suitable infrared absorber can be deposited. Since the sample is subjected to very high temperatures in a vacuum, the absorbing material must possess a low vapor pressure at high temperatures, and it must have a low reflectivity to infrared radiation. Tungsten is the only element which satisfies both criteria, and it was utilized for absorption experimentation.

The Drude-Lorentz theory of free electron absorption indicates that the deposited tungsten film must be at least 20 μm thick in order to absorb a fraction of the incident spectrum which is comparable to that for the case of bulk silicon. Tungsten films in excess of 1.5-μm thickness exhibit tensile failure when subjected to thermal cycling on an alumina substrate due to differential thermal expansion. Modest temperature increases have been observed for tungsten thicknesses less than 1 μm, but they are not sufficient to raise the surface temperature of alumina structures to 1000°C. A shift in the incident spectrum to blackbody radiation centered at 0.5 μm will increase absorption in alumina films by 20%, so increased surface temperature can be obtained in this manner.

It should be noted that a significant difference in surface heating of silicon and alumina SOI structures is not present in a conventional graphite strip heater. Samples in a strip heater rest on a large graphite thermal mass which is heated radiatively from a second graphite block. The SOI samples are in contact with this thermal mass, and they are heated conductively from the graphite block. This is in sharp contrast to an electron beam system, where energy must be absorbed radiatively, and the thermal mass of the system is the SOI sample itself.

2.3.3 Thermal Stress Considerations

Silicon-on-insulator samples are multilayer structures which are fabricated from materials which possess different thermophysical properties. The major constituents of our SOI topology for device fabrication are alumina, polysilicon and silicon dioxide. A composite of these materials is subjected to thermal cycling during ZMR, and this results in elastic strain within the composite layers and various stress levels within the SOI structure. These stress levels cause the composite structure to bend and assume a radius of curvature which is a function of geometric dimensions, the thermophysical properties of the substrate and those of the thin films. It has been experimentally observed that SOI structures on alumina substrates often thermally spall and exhibit mechanical failure as a result of high-temperature processing; whereas, SOI structures on silicon substrates do not exhibit this behavior with thermal cycling. This is the most significant impact of the use of an alumina substrate for ZMR processing of silicon. As a result, the thermoelastic properties of alumina have been investigated in detail.

The failure mode which has been observed in surface films on an alumina substrate at high temperatures has been tensile failure due to extremely high levels of strain in the thin surface films. In particular, it has been observed that 10-μm-thick (thick) polysilicon structures on alumina exhibit tensile failure prior to 1200°C, but 0.5-μm-thick (thin) polysilicon films on alumina do not suffer tensile failure and may be successfully recrystallized. Thick silicon films are desirable for fabrication of PIN diodes since epitaxial growth is otherwise necessary for the case of recrystallized 0.5 μm-thick films. To explicitly define this mechanical failure mode, all strain contributions within a typical SOI structure have been quantified to discern whether the failure of the thick films is due to high tensile stress levels or a secondary mechanism.

To evaluate the stress levels in each of the deposited films and the substrate, all strain contributions must be defined. The stress originates from intrinsic strain, pure bending strain and strain due to differential thermal expansion. Intrinsic strain is due to specific deposition parameters and is a property of the individual thin films. The magnitude of intrinsic strain is extremely small and can be neglected. Differential thermal expansion (DTE) strain is high due to the large mismatch in thermal coefficients of expansion, thereby dominating the stress level in each of the thin films and the substrate. Stress due to differential thermal expansion is uniaxially uniform within each deposited layer, with the magnitude in each layer dependent upon the magnitude of the thermal mismatch between the thin film and the substrate and the ratio of thin-film-to-substrate thickness. Non-uniform bending strain results from composite bending to relieve the differential thermal expansion strain. This results in a slight reduction in the total strain energy.

The most straightforward approach to calculating the stress profile of the composite is to assume that initially the layers are not joined together and they are bent to a radius R. If the layers are joined together such that point-by-point alignment is maintained at the interfaces, and the composite is bent to assume the same radius of curvature R, then the internal forces in the films must adjust to maintain coherency at the interface. Applying the strain boundary condition to an N-layer composite results in a linear system of N-1 equations which relate boundary strain due to differential thermal expansion to internal forces. This l near system is coupled to mechanical static equilibrium equations which relate moments and forces so that the stress can be determined in each layer. Fig. 2.5 is an illustration of a generic composite structure. Mechanical forces, moments, and radius are defined in the positive sense.

The above stress formulation was applied to SOI structures fabricated on alumina and silicon substrates. The numerical results of the calculations appear in Figures 2.6 and 2.7, and a detailed stress analysis appears in Appendix B. The most significant result of this analysis is the ability to

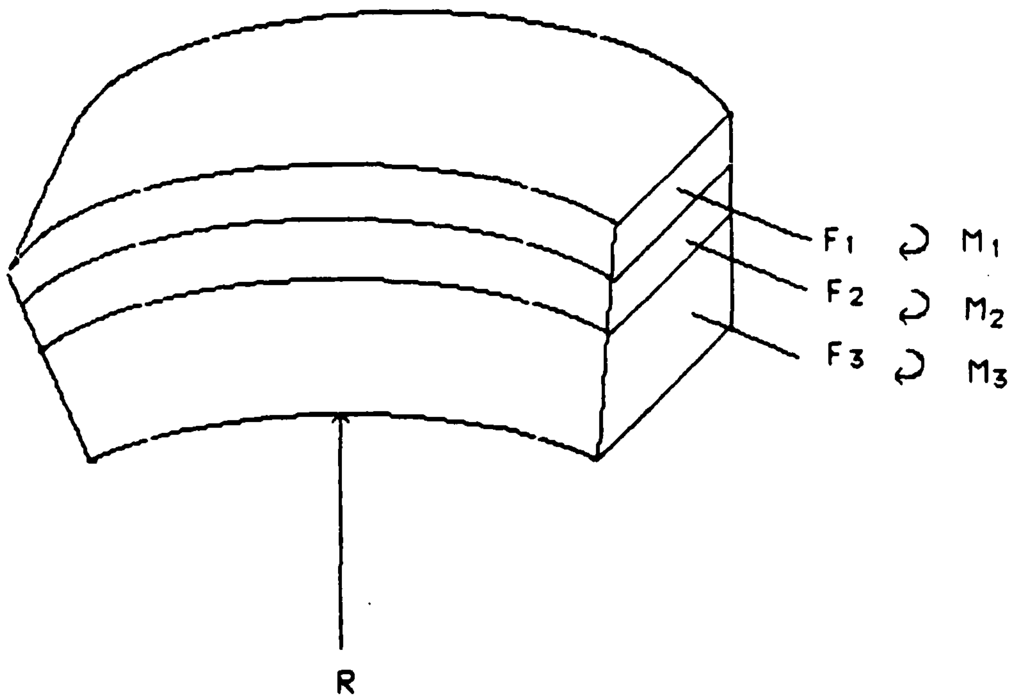


Figure 2.5 Sketch of a three layer composite used in stress analysis. Bending radius R, Forces F and Moments M are shown in positive sense.

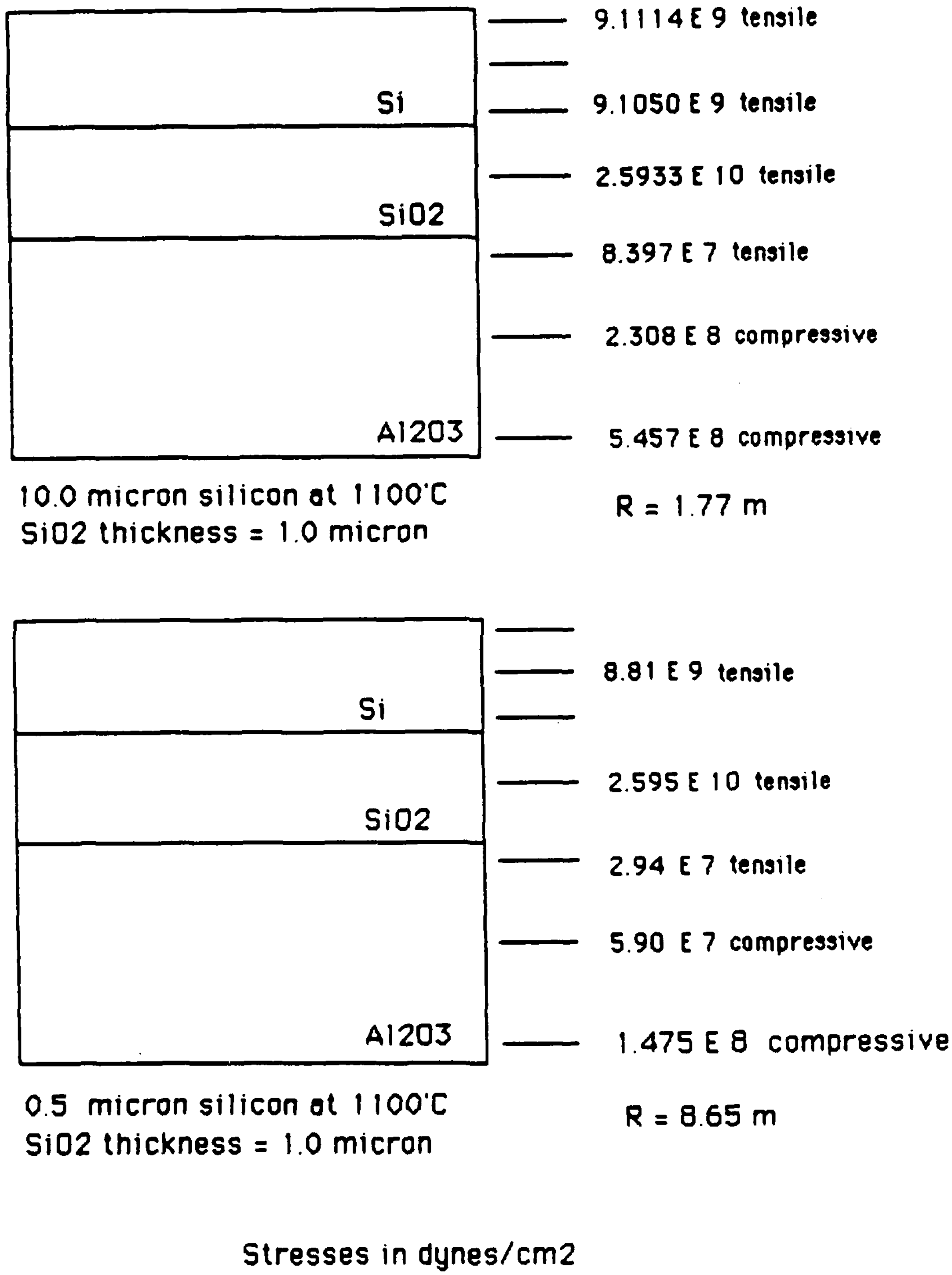


Figure 2.6 Comparison of stressess in Thick (10.0 micron) and Thin (0.5 micron) Silicon - on - Alumina

10.0 micron silicon at 1100°C

SiO2 thickness = 1.0 microns

R = 27.65 m

0.5 micron silicon at 1100 C

SiO2 thickness = 1.0 micron

R = 25.67 m

Stresses in dynes/cm2

Figure 2.7 Comparison of stresses in Thick (10.0 micron) and Thin (0.5 micron) Silicon - on - Oxidized Silicon quantify the amount of force that one layer of a composite structure can exert on another layer within the structure. The parameters which have the strongest influence on the magnitude of the exerted forces are the thin-film and substrate thicknesses and the difference between the thermal expansion coefficients of the composite materials. It has been concluded that the thickest member of the composite structure dominates the stress scenario since the magnitude of the exerted force is proportional to the ratio of film thickness to total composite thickness. Whereas this ratio is close to one for the substrate and close to zero for the thin surface films, it is evident that the substrate must dominate.

It is of particular interest to investigate the origin of the forces exerted on the polysilicon layer which is to be recrystallized. In an SOI topology on an alumina, the alumina substrate exerts extremely high tensile forces on the polysilicon layer since the alumina is five hundred times thicker than the polysilicon, and the thermal mismatch is approximately six ppm. Within an SOI topology on a silicon substrate, the substrate is still five hundred times thicker than the polysilicon, but no DTE force is exerted by the substrate on the polysilicon because the thermal mismatch is zero. Thus, in an SOI structure on a silicon substrate, only the thin silicon dioxide layers can exert DTE forces on the polysilicon, so the stress levels are modestly low. The net effect of an alumina substrate on the stress level in the polysilicon at high temperature can be inferred from Figs. 2.5 and 2.6. These data show that the tensile stress values in polysilicon-on-alumina substrates are two orders of magnitude greater than those for a silicon substrate. The only stress relief mechanism present in the SOI structures is bending, but calculations indicate that the stress relief due to bending is three orders of magnitude below that of differential thermal expansion, so they can be ignored.

Numerical calculation of the tensile stress level at high temperature in 10.0-μm-thick polysilicon and 0.5-μm-thick polysilicon indicates that the stress level in the thick film exceeds that of the thin film by less than 5%. Thus, high tensile stress cannot be utilized to explain the tensile failure of the thick films and the structural integrity of the thin films. However, there is a secondary mechanism involved which is a strong function of the film thickness. This mechanism incorporates deadherence forces which are normal to the substrate/thin-film interface. The magnitude of the deadherence force increases as the thickness of the film is increased, and eventually the magnitude exceeds a critical value. This deadherence mechanism is local and usually occurs at imperfections in the CVD films at the substrate interface. The local deadherence perturbation is acted on by large tensile forces which initiate tensile failure. Thus, for a given value of average stress, there exists a critical thickness which cannot be exceeded if deadherence is to be avoided. Since this parameter is material and process dependent, it must be determined experimentally.

2.3.4 Mechanical Strength Considerations

It has been experimentally observed that the mechanical properties of alumina substrates are much different than those of silicon substrates. Alumina is a brittle, ceramic material which does not possess any plastic flow mechanisms. Silicon is a ductile material which can relieve imposed strains by plastic flow mechanisms such as dislocation formation and glide/slip processes. These mechanical properties have a significant impact on the recrystallization of silicon, primarily in regard to strain relief. These parameters also define the maximum temperature gradient which can be imposed upon the SOI structures if one is to avoid mechanical failure during the application of the primary heat source for recrystallization.

As mentioned earlier, the SOI composite structures are composed of materials which possess different thermophysical properties, and as a result, thermal strains are induced into the films during temperature cycling. These strains can be reduced by several mechanisms, the most dominant of which is bending. The amount of strain relief which can occur for a given strain level is determined by the flexural characteristics of the substrate. Alumina has a Young's modulus which is three times that of silicon. As a result of this stiffness, the alumina will not provide as much bending strain relief as a silicon substrate. Stated in a different manner, for a given average stress value within the surface films of the composite, the silicon substrate will provide enhanced strain relief due to bending.

A second mechanism of strain relief is that of plastic flow. If the strain levels at the surface of the silicon substrate approach one-ten thousandth of the shear modulus, dislocations are formed which relieve strain energy. If the strain levels approach one one-hundredth of the shear modulus, slip processes relieve strain energy. These two mechanisms of strain relief a·e not available in the alumina system since alumina does not undergo any plastic flow. Thus, not only is the magnitude of the stress two orders of magnitude higher in the alumina system, it possesses no means for strain relief other than fracture.

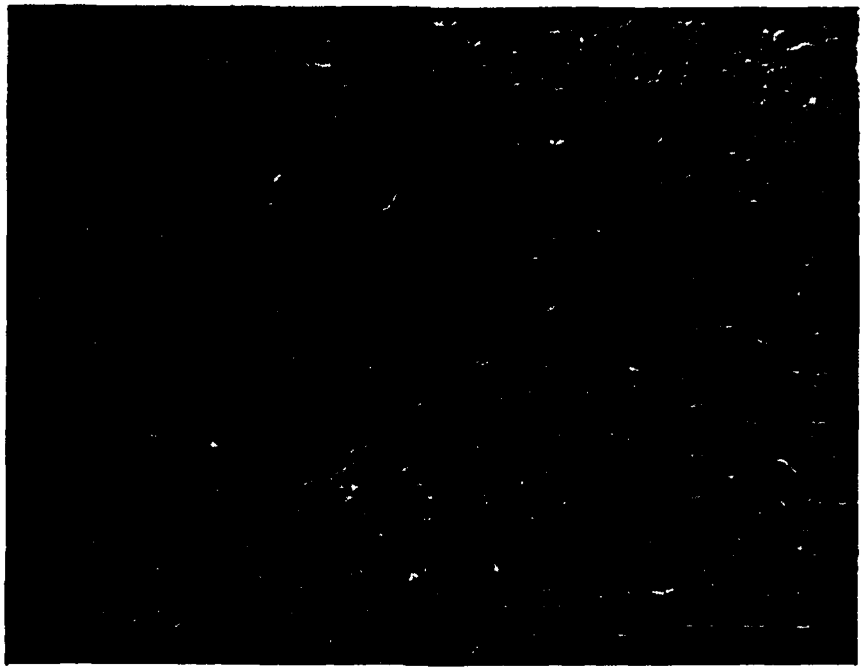
The mechanical properties of alumina also define the maximum temperature gradient which can be imposed upon the SOI sample during ZMR. Since alumina is brittle, the resistance to thermal shock failure can be approximated by Young's modulus divided by the linear coefficient of expansion. The coefficient of expansion is a function of temperature, so the maximum thermal gradient is also a function of temperature. At recrystallization temperatures, the maximum temperature gradient which can appear across an SOI sample is about 400°C. If an alumina SOI sample is to be recrystallized by means of an electron-beam or a graphite strip heater, the substrate bias temperature must be at least 1000°C to avoid fracture due to thermal shock. There is no such limitation for an SOI structure on a silicon substrate.

2.3.5 Stress Relief Considerations

A method of alleviating the tensile stress in a polysilicon film over alumina is to thermally match the surface of the alumina substrate to the expansion coefficient of silicon. This can be accomplished by the formation of an interphase compound of alumina and silicon dioxide. If the surface compound has a crystalline structure similar to the constituent phases, one can expect the compound to possess a thermal coefficient of expansion between the extreme values of the individual constituents. In the case of alumina and silicon dioxide, the coefficient of expansion of such a compound would be between 0.4 and 10.0 ppm. Since silicon has an expansion coefficient of 2.6 ppm, a thermal match is feasible. The formation of an interphase compound was accomplished by high temperature annealing of a 2-μm-thick CVD silicon dioxide film on alumina. These structures were then annealed at 1550°C in an oxygen overpressure. The temperature of 1550°C was selected to avoid the first liquidus point for the alumina silica system. This provided control over the formation of interphase compounds.

Figure 2.8 shows SEM photographs of samples subjected to the high-temperature anneal. They indicate that a surface phase consisting of a very-large-grained morphology has been formed. Cross-sectional SEM photographs indicate that this is a true surface phase, since no crystallites are apparent in the bulk alumina. Strain relief via thermal expansion matching varies lin-

A



B

Figure 2.8: SEM Photographs of CVD Silicon Dioxide on Aluminum after 1500^{o}C Anneal in Oxygen Overpressure

A. Interphase Crystallites at 1000X.

B. Typical Crystallite at 5000X.

early with the difference between surface-phase and bulk-alumina expansion coefficients, so order-of-magnitude reduction in stress can be expected. Further work is underway to obtain a continuous surface phase and to discern the relative concentrations of the constituent species.

Viscoelastic strain relief is an extremely effective method of strain relief. It can be utilized in an SOI structure by the incorporation of a phosphosilicate glass layer into the SOI composite. PSG exhibits a temperature-dependent viscosity which can be utilized to relieve stress via a velocity/flow mechanism at high temperatures. PSG viscosity is 10^{19} Poise at room temperature (solid), but it is below 4×10^7 Poise at temperatures typically used in ZMR processing. The value of 4×10^7 Poise is defined as the universal softening point for glass materials, hence the PSG is a viscous liquid at high temperature and substantial flow can occur within the PSG. If a PSG layer is incorporated into the SOI structure between the polysilicon and the alumina substrate, a temperature-dependent stress relief mechanism will result, and the stress in the polysilicon can be reduced significantly. The strain energy in the polysilicon is converted to kinetic flow in the PSG. If the alumina SOI structure is treated as a lumped-parameter deterministic system, calculations indicate that the time constant for four-order-of-magnitude stress relief in the polysilicon film at ZMR substrate temperatures is on the order of three minutes. Thus, a three-minute <u>in situ</u> anneal of alumina PSG SOI structures prior to ZMR will reduce the stress in the surface films by about four orders of magnitude. This stress level is below that of conventional SOI structures on silicon substrates. The polysilicon film is essentially "floating" on the alumina substrate during recrystallization.

It should be noted that the effect of static stress levels prior to recrystallization on the origin of subgrain boundaries has not been quantified by investigators in the ZMR field. The PSG strain relief layer represents an excellent vehicle for the evaluation of the effect of static stress on subgrain boundary formation. SOI structures on alumina substrates containing a PSG viscoelastic strain energy absorption layer represent our most recent phase of SOI experiments, and these experimental results are reported in detail in Chapter 3.

3. SILICON-ON-ALUMINA RECRYSTALLIZATION RESULTS

In this Chapter the key recrystallization results obtained with silicon-on-alumina to date are presented. While device-quality films are not yet demonstrated, we believe that the latest results are quite promising. When combined with the supporting analytical effort, the directions to obtain PIN-diode-quality films are developed.

Polysilicon films have been recrystallized on alumina substrates utilizing a graphite strip heater. A current sample topology of a SOI structure on an alumina substrate appears in Figure 3.1. The sample consists of a 500-µm-thick alumina substrate, a 1.0-µm-thick CVD silicon dioxide sublayer, a 0.5 µm-thick polysilicon layer and a 1.0-µm-thick CVD silicon dioxide capping layer. The sublayer prevents the molten silicon from making contact with the alumina substrate, and the capping layer aids in confinement of the molten zone to prevent agglomeration. The polysilicon layer receives a double implant of nitrogen to ensure nitrogen incorporation at both polysilicon silicon- dioxide interfaces. Nitrogen fluences in the range of 1 to 5 x 10^{15} cm^{-2} ensure that the molten silicon wets the silicon dioxide.

A set of graphite strip-heater recrystallization parameters have been determined which result in high-quality single-crystal silicon-on-alumina films. A substrate bias temperature of 1150°C is sufficient to avoid thermal shock failure of the alumina substrate and prevent thermal spalling of the surface films. An upper strip power of approximately 1600 W and a zone translation speed of 100 µm/sec result in agglomeration-free recrystallization. The molten zone is 700 µm wide. In situ video monitoring of the molten zone was employed to characterize the liquid-solid interface and to discern the effect of various liquid-solid interface geometries on the resulting crystal morphology. The interface geometry which resulted in the most stable crystal growth

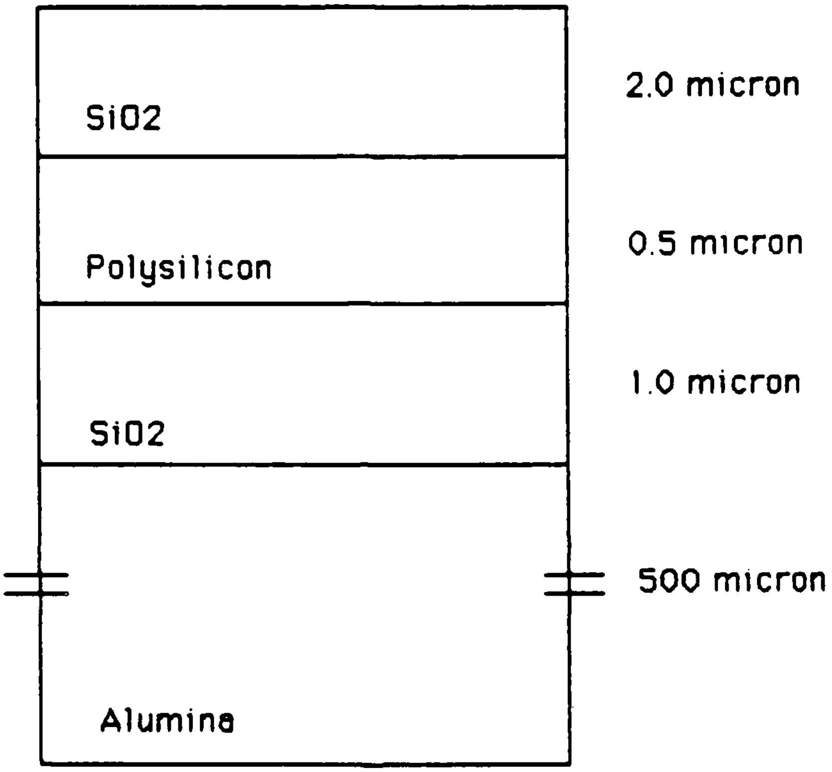


Figure 3.1 Typical SOI composite

bordered between primary dendridic and cellular geometries. An unusually persistent partial melting phenomenon was observed during the zone-melt recrystallization. This can be attributed to the high static stress levels within the polysilicon film. Careful control of the process parameters significantly reduces the severity of the partial melting effect.

After recrystallization, the silicon-on-alumina samples were examined with a Nomarski contrast microscope to investigate the predominant defect structures. The vast majority of defects which cause surface perturbations across the recrystallized films are attributable to grain pullout defects from the alumina substrate or the formation of silicon nitride crystallites. The surface undulations which are caused by grain pullouts are clearly evident in Figure 3.2A, a low-magnification Nomarski photograph of a recrystallized film. Silicon nitride crystallites are formed due to the presence of a large concentration of ion-implanted nitrogen. Silicon nitride preferentially phase segregates in a molten silicon matrix resulting in a second-phase defect in the recrystallized film. The formation of the silicon nitride phase is kinetically controlled and is a function of melt dwell time. The formation of silicon nitride defects can be reduced considerably by increasing the molten-zone translation speed.

Hillock formation is also observed in recrystallized silicon-on-alumina films. This is attributed to partial melting of polysilicon in the vicinity of the molten zone. These silicon pools freeze into a solid silicon matrix, with volume expansion upon solidification resulting in hillock formation. Localized strain fields due to alumina surface roughness also contribute to hillock formation.

The recrystallized silicon-on-alumina films were subjected to extensive characterization to determine the crystallographic texture of the silicon

A

B

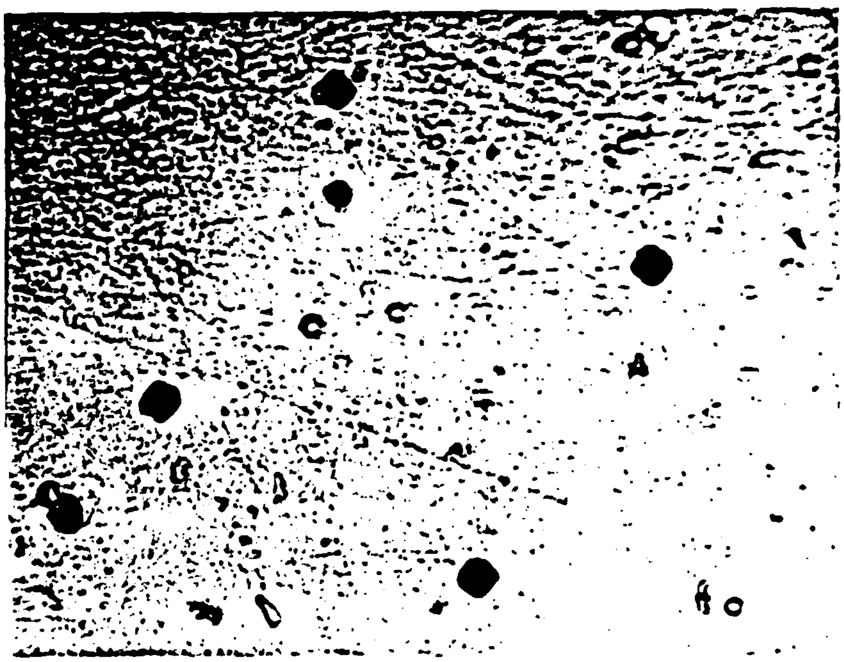


Figure 3.2: Silicon-on-Alumina Film Texture

A. Optical Photograph (80X)

B. Metallograph of Etch Pits Indicating (100) Texture film. Diffractometry and etch-pit analyses were utilized to discern the direction of the surface normal for the film and the in-plane film orientation.

The etch-pit technique utilizes a wet chemical anisotropic etch to delineate the (111) planes of the silicon film and provide an indication of film texture and in-plane orientation. After recrystallization, the sample capping layer is removed and a new CVD silicon dioxide layer is deposited onto the surface of the recrystallized silicon film. An etch-pit pattern consisting of 4-μm-diameter openings on 50 μm centers is transferred to the silicon dioxide layer using photolithographic techniques. The silicon dioxide is etched from the 4-μm openings with buffered hydrofluoric acid. The remaining oxide serves as an etch barrier to the selective etch. After a KOH n-propanol etch, the geometry of the pits beneath the openings reflects the symmetry of the silicon film. For our films (as in the experiments of others), the pits appear as squares. This indicates that the silicon surface has four-fold symmetry and the texture is (100). The diagonal of a square etch pit indicates the <100> direction, and for our silicon-on-alumina samples this direction is coincident with the direction of molten-zone motion. Figure 3.2a shows an 80X optical photograph of recrystallized silicon-on-alumina sample, and Fig. 3.2B is a 1000x metallograph of etch pits in silicon-on-alumina which indicates the (100) texture. The line defects evident in Fig. 3.2b are the polishing scoring lines on the alumina substrate.

An x-ray analysis was performed to determine the surface plane orientation of the recrystallized silicon-on-alumina. Double crystal diffractometry was employed to study the texture of the films, but the diffracted intensity was too low for analysis. The extinction depth of CuK_{α} radiation in silicon is approximately 50 μm, while the thickness of the silicon film is only 0.5 microns. Thus, the diffracted intensity should be extremely low because the

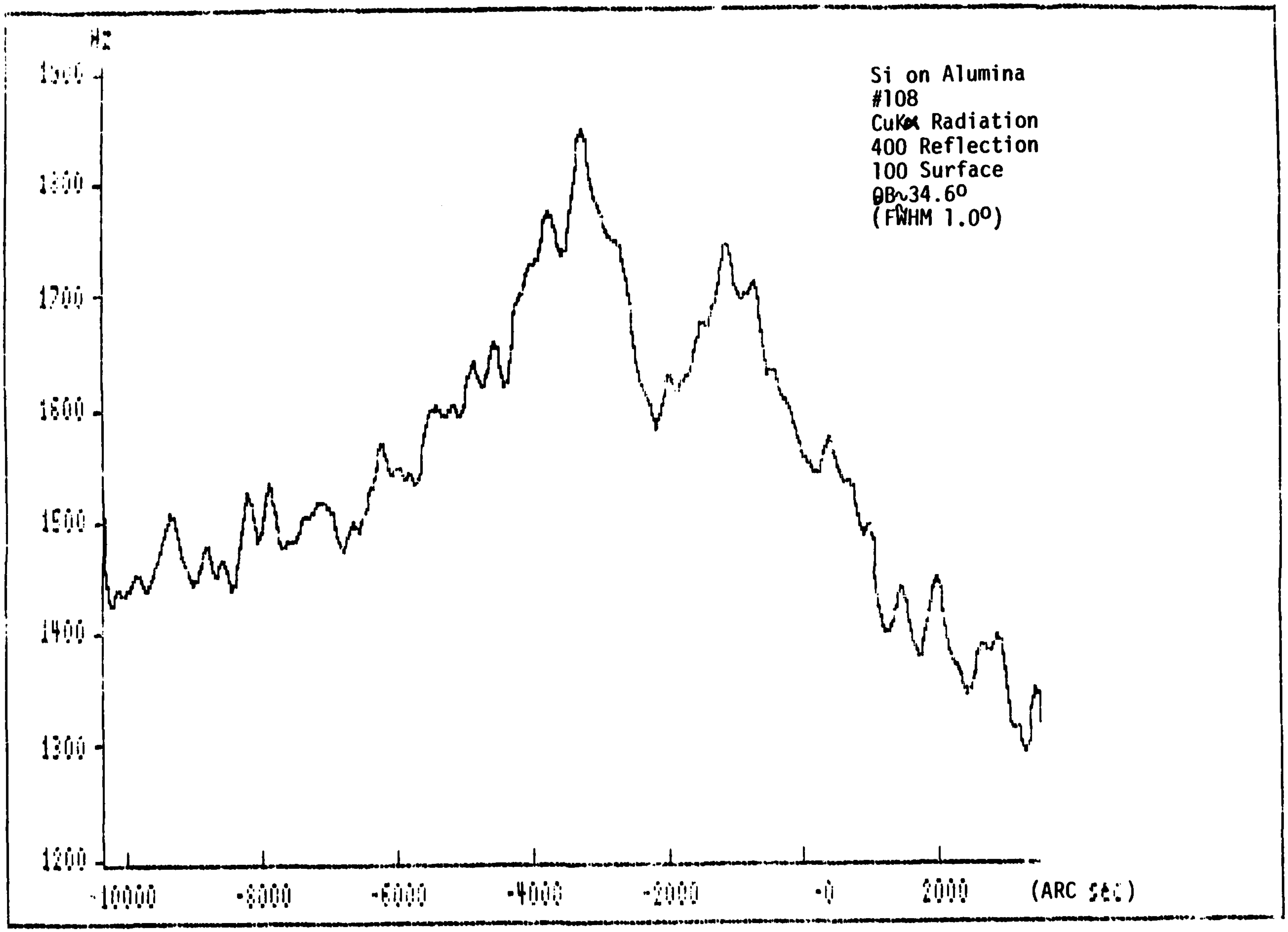


FIGURE 3.3: Single Crystal Diffractometer Intensity of Silicon-on-Alumina Film

volume of recrystallized silicon is only a fraction of the extinction volume. This, coupled with the loss in the first crystal of the double crystal diffractometer, was responsible for the low diffracted intensity. To alleviate this problem, the first crystal was removed and the diffractometer was used in a single-crystal mode.

Figure 3.3 is a plot of diffracted intensity versus angle for the recrystallized film. Full width at half maximum for the plot is less than 1^o and centered at the expected (100) peak. The double maximum indicates that the specific area under analysis contains a low angle grain boundary. No peaks were present at either (110) or (111) angles. The x-ray analysis confirms that the orientation of the plane normal to the silicon-on-alumina surfaces is in the <100> direction.

The polysilicon film is subjected to very high tensile stress when the temperature of the SOI composite is increased, and the recrystallized silicon film is subjected to very high compressive stress upon cooling. Failure of the polysilicon films due to both tensile and compressive stress has been observed. The occurrence of these failure modes is statistical in nature, as with all fracture processes. High levels of static stress within the recrystallized film also contribute to hillock formation and partial melting phenomena.

The stress in the polysilicon (or single-crystal silicon) is controlled by the substrate alumina, so the effect of the substrate must be removed to reduce the stress in the films. This has been accomplished through the use of a "soft glass" sublayer. Incorporation of a soft glass sublayer into the SOI sample composite effectively decouples the substrate and the surface films at high temperature. Phosphosilicate glass has been utilized as a soft glass sublayer. Figure 3.4 illustrates an alumina SOI composite with PSG sublayer

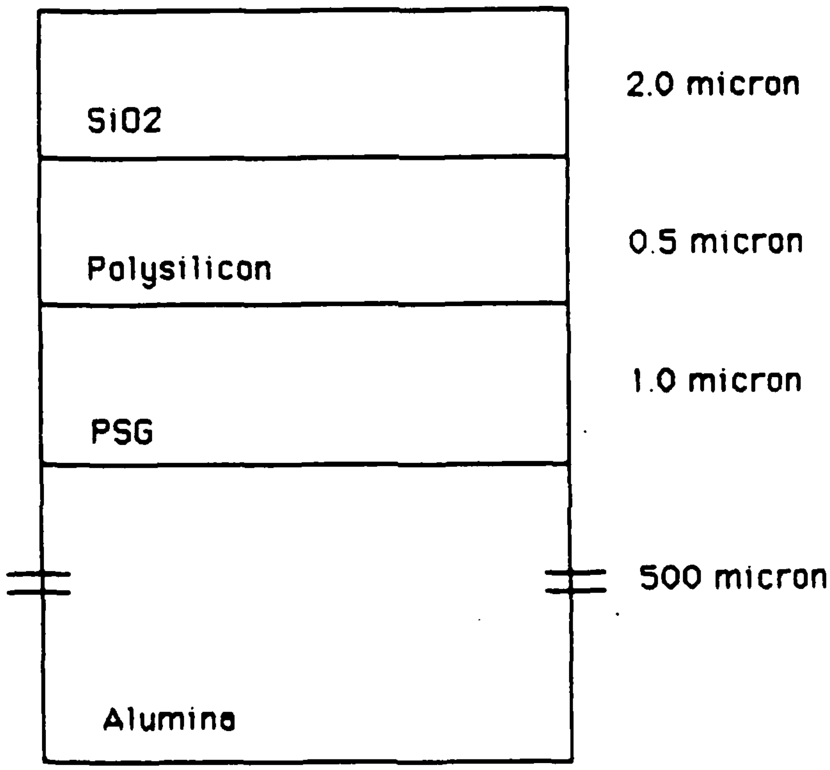


Figure 3.4 SOI composite structure with PSG sublayer

incorporated into the structure. These samples consist of a 500-μm-thick alumina substrate, 1.0-μm-thick 8wt% PSG sublayer, 0.5-μm-thick polysilicon layer, and 2.0 μm-thick CVD silicon dioxide capping layer. An additional sample with a 10-μm thick polysilicon layer but otherwise identical to the other was included. Recently these samples, along with our "conventional" sample (SiO_2 instead of PSG) were recrystallized.

The recrystallization results confirmed the difficulty in maintaining film integrity without the PSG layer, although very small recrystallized regions were obtained. The thickness of the PSG layer was only marginal, so one 0.5-μm-thick polysilicon sample maintained good adherence over the entire 1-inch-square area while the other exhibited compressive failure during cooling after recrystallization. These results are quite encouraging, since they are compatible with stress calculations and demonstrate the validity of the PSG layer for strain relief.

The 10-μm-thick polysilicon cracked, but the recrystallized regions were relatively large (approximately 1000-μm^2 area). The recrystallized regions appear to be of high-quality, based upon visual inspection, but detailed analysis has not been performed at this time.

Supporting calculations indicate that increasing the PSG thickness to 3-μm and patterning the films into islands with 300-μm by 300-μm dimension will provide enhanced strain relief and improved adherence. We expect a significant improvement in electrical quality as well. This logical extension of our present program is expected to result in device-quality films.

While the electron-beam recrystallization results have not been as promising to-date, we have included results obtained in Appendix C for completeness. Note particularly the potential advantage in island recrystallization using electron-beam heating.

4.0 SURFACE-ORIENTED SILICON PIN DIODES

While we realized that PIN diodes on recrystallized silicon would be difficult to achieve during this initial two-year program, it was important to guide the recrystallization effort with device constraints. In this Chapter, a brief technical overview of PIN parameters and device design perspective is presented (Section 4.1), followed by the processing sequence and mask design of the PINs with test structures (Section 4.2). Then we describe the processing steps and fabrication procedures, with emphasis on particularly critical and/or novel procedures (Section 4.3). In conclusion, the initial results obtained with surface-oriented-PIN diodes on single crystal silicon substrates are presented (Section 4.4).

4.1 Technical Background and Diode Design

The First-Year Annual Report included a complete section on PIN design[1] (Chapter 4). We indicated that a lateral device structure was preferred over a vertical topology in order to achieve contacts with low parasitic spreading resistance. In addition, the lateral device is more compatible with monolithic integration. The key disadvantages of the lateral device is that the PIN diode figure-of-merit is reduced due to non-uniform injection in forward bias and excess parasitic capacitance. Device power handling is also reduced. For the applications envisioned, reasonable diode performance is anticipated if:

1. adequate carrier lifetime is obtained in the recrystallized film.
2. reasonably uniform injection can be achieved in forward bias from the device structure.

Having selected the lateral device, and realizing that lifetime is a key question for our epi-layer grown on recrystallized silicon, we explored device structures and dimensions to arrive at our final designs. Three lateral device structures were considered as depicted in Fig. 4.1, namely the surface-oriented, the pocket and the mesa structures. As demonstrated by Battershall and Emmons,[(21)] a deep pocket structure can provide injection characteristics which are intermediate between an optimum vertical design and the surface-oriented structure (a conventional lateral device completely compatible with standard Si IC fabrication).

Assuming that the effective I-layer width (W) is sufficiently short compared to the ambipolar diffusion length (L_A), i.e. $W < 2L_A$, the intrinsic layer resistance (R_I) under forward bias can be expressed as:

$$R_I = \frac{W^2}{2\mu A \tau_{eff} I_f}$$

where μ_A is the ambipolar mobility (~600 $cm^2/Vsec$), I_f is the DC forward bias current and τ_{eff} is the effective lifetime. The effective lifetime can be expressed as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{A,B}} + \frac{1}{\tau_{A,S}} + \gamma\, n^2$$

where $\tau_{A,B}$ is the bulk ambipolar lifetime, $\tau_{A,S}$ is the effective surface lifetime and γ is the Auger recombination coefficient for silicon (~3×10^{-31} cm^6/sec).

Bipolar transistors fabricated in recrystallized silicon-on-oxidized-silicon (i.e. $Si/SiO_2/Si$) have resulted in current gains which are compatible with 10-nS recombination lifetime[22]. While Si-on-alumina (Si/Al_2O_3) or Si-on-PSG-on-alumina ($Si/PSG/Al_2O_3$) would be expected to have more defects, at least at the early stages of development, an epi-layer grown over the recrystallized silicon is expected to have improved lifetime due to impurity gettering if the recrystallized film is phosphorus doped. An ambipolar lifetime in the range

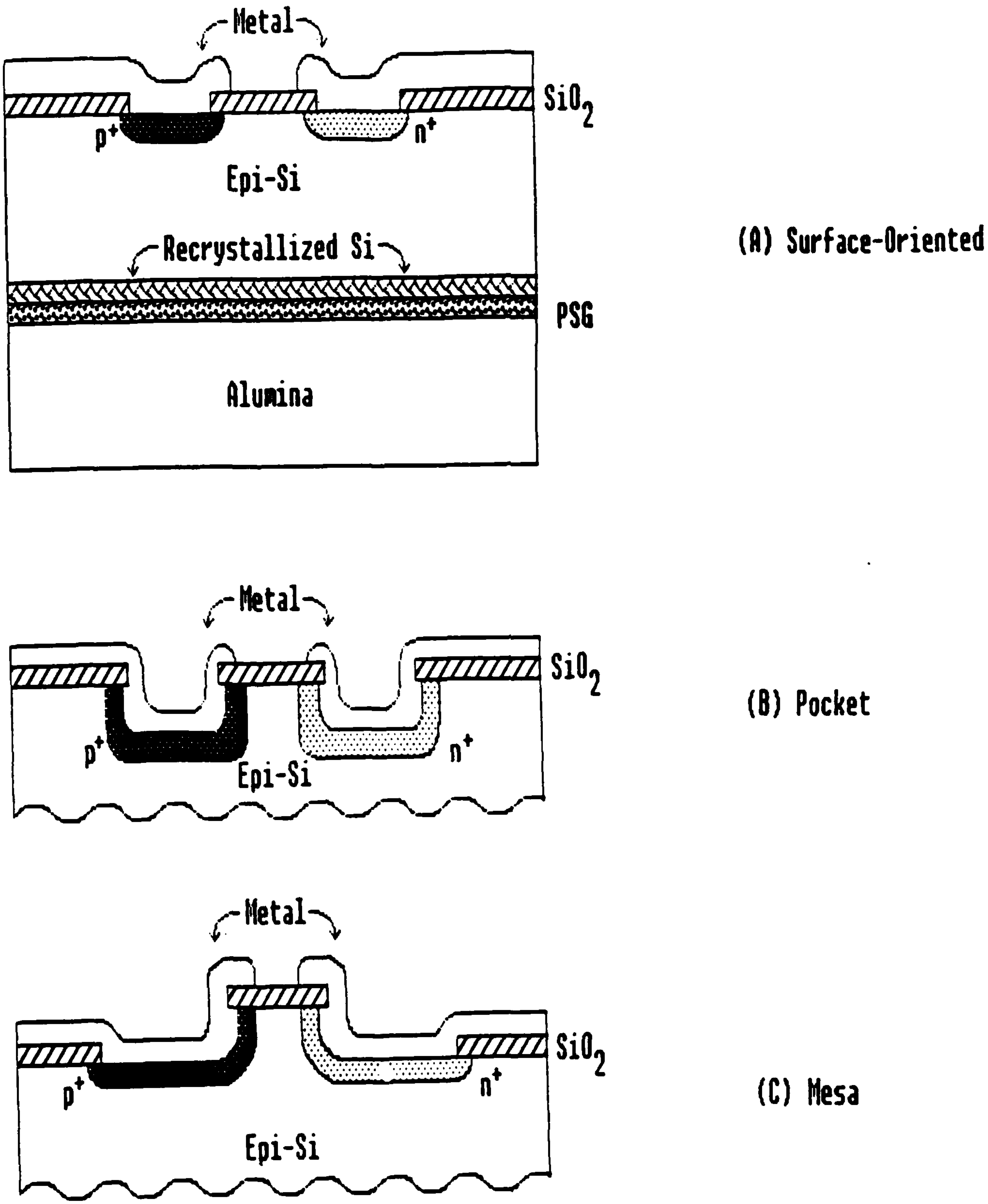


Figure 4.1: Lateral PIN Diode Structures

of 5 to 80 nS is anticipated with a mature technology, and 20 nS is being used for nominal design purposes.

All device structures being considered have the I-layer surface passivated with a thermally grown oxide so that surface recombination is not expected to be a concern with these ranges of bulk lifetime. With 20-nS bulk ambipolar lifetime, electron concentrations of 4 to 8 x 10^{18} cm^{-3} result in only a 10 to 25% reduction in effective lifetime due to Auger recombination.

When these two relationships are combined with the principle of charge control, namely

$$I_f = \frac{qnAW}{\tau eff}$$

the key device parameters can be obtained, with representative values given in Table 4.1. The need to keep the lifetime above 10 nS in order to obtain low forward-bias resistance with reasonably sized intrinsic layers is apparent.

In considering more detailed implementations of the deep etched structure (of Fig. 4.1), two alternatives, the pocket (4.1B) and the mesa (4.1C), become apparent. The first method involves etching two pockets into the silicon: one for the p+ diffusion and the other for the n+ diffusion. The second method etches most of the silicon surface, leaving a small mesa for the device. Because the intention was for both processes to yield a device height on the order of 5 μm, the problem of step coverage both in earlier processing and with aluminum metallization must be considered.

The solution proposed was to make contact to the device with doped polysilicon (see Section 4.2). Besides acting as contacts to the device, the doped polysilicon can be used as the diffusion sources needed to form the p+ and n+ regions. The dopants can be introduced in a very controllable fashion by ion implantation into the polysilicon after deposition. It is critical

$\tau_{A,B}$ (nS)	L_A (μm)	W_{max} (μm)
5	2.8	5.6
20	5.6	11.2
80	11.2	22.4

with $\tau_{A,B}$ = 20 n S and I_f = 10 mA

W (μm)	R_I (ohms)
5	1.0
10	4.0
15	9.0

with $\tau_{A,B}$ = 5 n S and I_f = 10 mA

W (μm)	R_I (ohms)
2	.65
4	2.6
6	5.8

Table 4.1: Representative PIN Diode Parameters

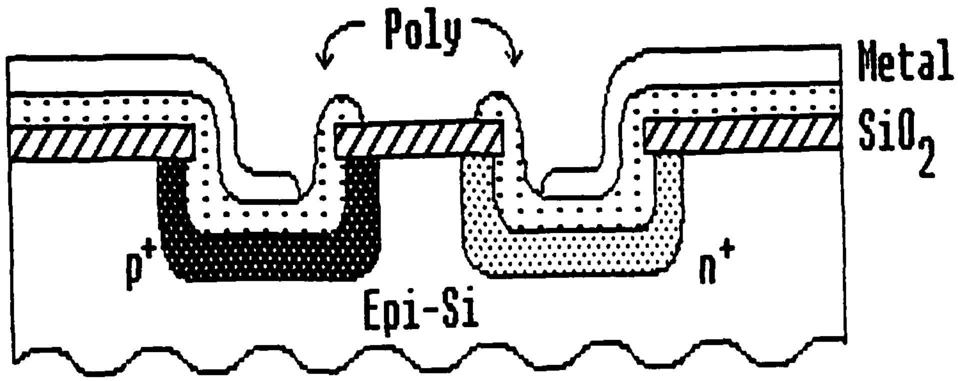
that the polysilicon deposition be conformed so that the deep side walls are covered. A low-pressure chemical vapor deposition (LPCVD) system allowed us to put down highly uniform layers of polysilicon, resulting in a device structure shown in Fig. 4.2.

One potential difficulty is that the polysilicon covering the crucial sidewalls will not be implanted. Since the diffusion coefficient of the dopant in polycrystalline silicon is much greater than that in the bulk material, we expect that an initial lack of sidewall impurity incorporation will not be critical. That is, during the diffusion process, the dopants should first redistribute evenly in the source and provide uniform p and n regions.

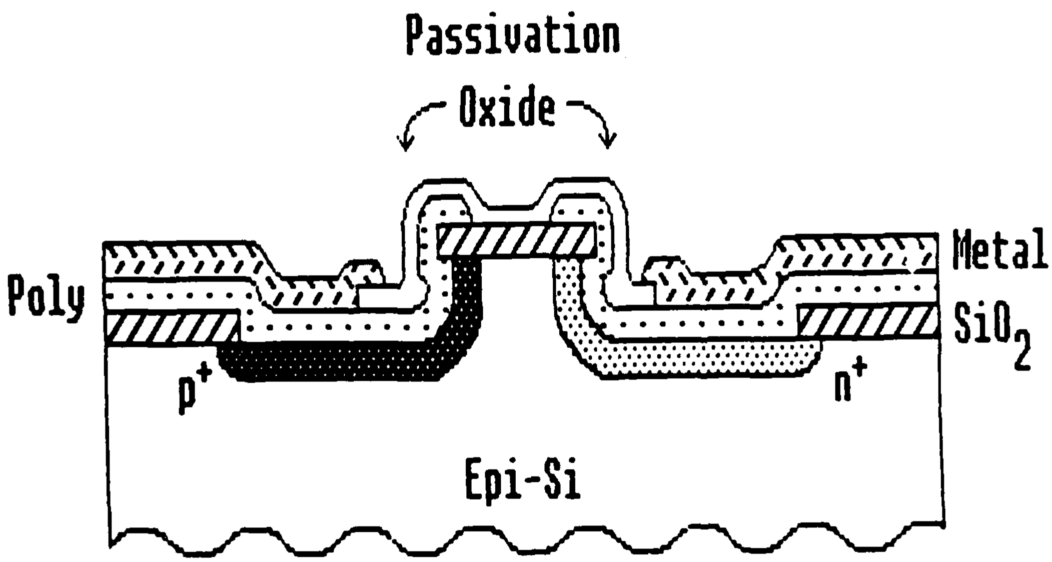
Returning to the selection between the pocket and mesa structures, the parasitic series resistance was considered to be the deciding factor. While polysilicon is adequate for many MOSFET gates, its resistivity is sufficiently high so that the parasitic contact resistance can be detrimental. For the contacts on each side of the diode, the pocket structure requires at least an additional 5 µm length of polysilicon over that for the mesa structure . This is due to the extra step of sidewall opposite that contacting the device, and this must also be covered by LPCVD polysilicon since the metallization layer cannot extend beyond the step. First-order calculations indicate that the additional series resistance for the pocket structure may be as high as 1-3 ohms. Thus, the mesa has a significant advantage, although the resistivity of the polysilicon on each side of the mesa is still an important design consideration.

4.2 Processing Sequence and Mask Set Design

With the device structure finalized, the actual processing sequence was selected and experiments were planned to ensure that key fabrication steps could indeed be implemented prior to final mask design. An outline of the ma-



(A) Pocket



(B) Mesa

Figure 4.2: Detailed Cross-Section of Pocket and Mesa Structures

jor steps is included in Table 4.2 and an explanation of key processes follows.

The step referred to as an RCA clean is performed prior to oxide growth to remove any contaminants. The sample is immersed in heated solutions of HCl/H_2O_2/DI water and NH_4OH/H_2O_2/DI water followed by a thorough rinsing. The thermal oxidation provides a SiO_2 surface that not only is needed for the deep mesa pattern transfer step, but a surface which also must provide a low surface recombination velocity for PIN forward bias operation.

The etching of silicon to form the mesa structure is performed by plasma or reactive ion etching in order to achieve a good degree of anisotropy. An Applied Materials 8100 hexode plasma etcher was used. Experiments were conducted with CF_4/O_2, CHF_3/O_2, SF_6/O_2 and SF_6/Ar plasmas.

After the crucial etching step (discussed further in Section 4.3), a uniform layer of silicon nitride is deposited by LPCVD to serve as an active-area mask during field-oxide (LOCOS) growth. In the same step, we passivated the exposed end sidewalls of the mesa by allowing the same oxide growth. (Every effort must be made to clean the surfaces prior to oxidation.) Afterwards, the nitride is plasma etched to expose the active region for further processing. Following polysi .icon deposition (as described earlier), the p+ and n+ injecting contacts are implanted with the depth controlled by a prudent choice of energies. We used 80-keV BF_2^+ for the p+ (boron) implant, followed by 60-keV P+ for the n+ (phosphorus) implant. The actual diffusion is accomplished by a combination oxidation/drive-in so that the desired I-region thickness is obtained. The polysilicon is then patterned by a photolithography step and plasma etch. The final few steps of oxide etch, aluminum evaporation and patterning are straightforward.

TABLE 4.2

Processing Steps for Mesa PIN Diode

1. Characterize starting material
2. RCA clean
3. Thermal oxidation
4. Spin coat and pattern photoresist: mask level 1
5. Oxide etch (plasma)
6. Plasma etch silicon
7. LPCVD silicon nitride and pad oxidation
8. Apply and pattern photoresist: mask level 2
9. Plasma etch exposed silicon nitride and pad oxide
10. RCA clean
11. Field oxidation
12. Plasma etch remaining silicon nitride and pad oxide
13. LPCVD polysilicon
14. Apply and pattern photoresist: mask level 3
15. P+ implant
16. Apply and pattern photoresist: mask level 4
17. N+ implant
18. Apply and pattern photoresist: mask level 5
19. Plasma etch polysilicon
20. Anneal/drive-in (oxidation)
21. Remove oxide (for contact preparation)
22. Aluminum evaporation
23. Apply and pattern photoresist: mask level 6
24. Aluminum etch
25. Sinter and anneal

Based upon this processing sequence, the mask design for individual devices was developed as shown in Fig. 4.3. Note that for illustration purposes the device dimensions are not to scale. The actual dimensions of the devices were varied to allow evaluation of the electrical properties of the recrystallized material. In particular, a range of I-region thicknesses is necessary to separate effects of bulk and surface recombination and to quantify material parameters. In order to characterize the various areas of the sample, a die size allowing a single section on each die for test structures with good device coverage is needed. A basic chip size of 600 x 600 μm^2 was selected as a compromise with 1-inch-square alumina substrates.

The reduced chip area limits the number of devices which can be tested at microwave frequencies to six because of the long metal lines which are necessary to provide access to the diodes and to allow a good connection to the test fixture (a Cascade microwave probing system was not available). These lines must be spaced sufficiently to prevent coupling. All six devices have the same width but have varied I-region dimensions, values which were chosen based on both lifetime and processing considerations. There are one each of 6- and 48-µm I-region thicknesses, and two each of 12- and 24-µm thicknesses. The latter devices have a higher probabil.ty of giving good yield and electrical results. A plot of the mask layout is included in Fig. 4.4.

The space between the microwave-testable devices has been used for devices which can be probe tested for DC and low-frequency characterization. These too have I-regions in the four denominations listed above, and they are arranged such that each type is well distributed over the substrate so as to provide information on the uniformity of the I-layer material. In total, there are 35 DC devices (five rows of seven). In addition, there are two sets of 12- and 24-µm diodes which have varying widths from a base value of 150

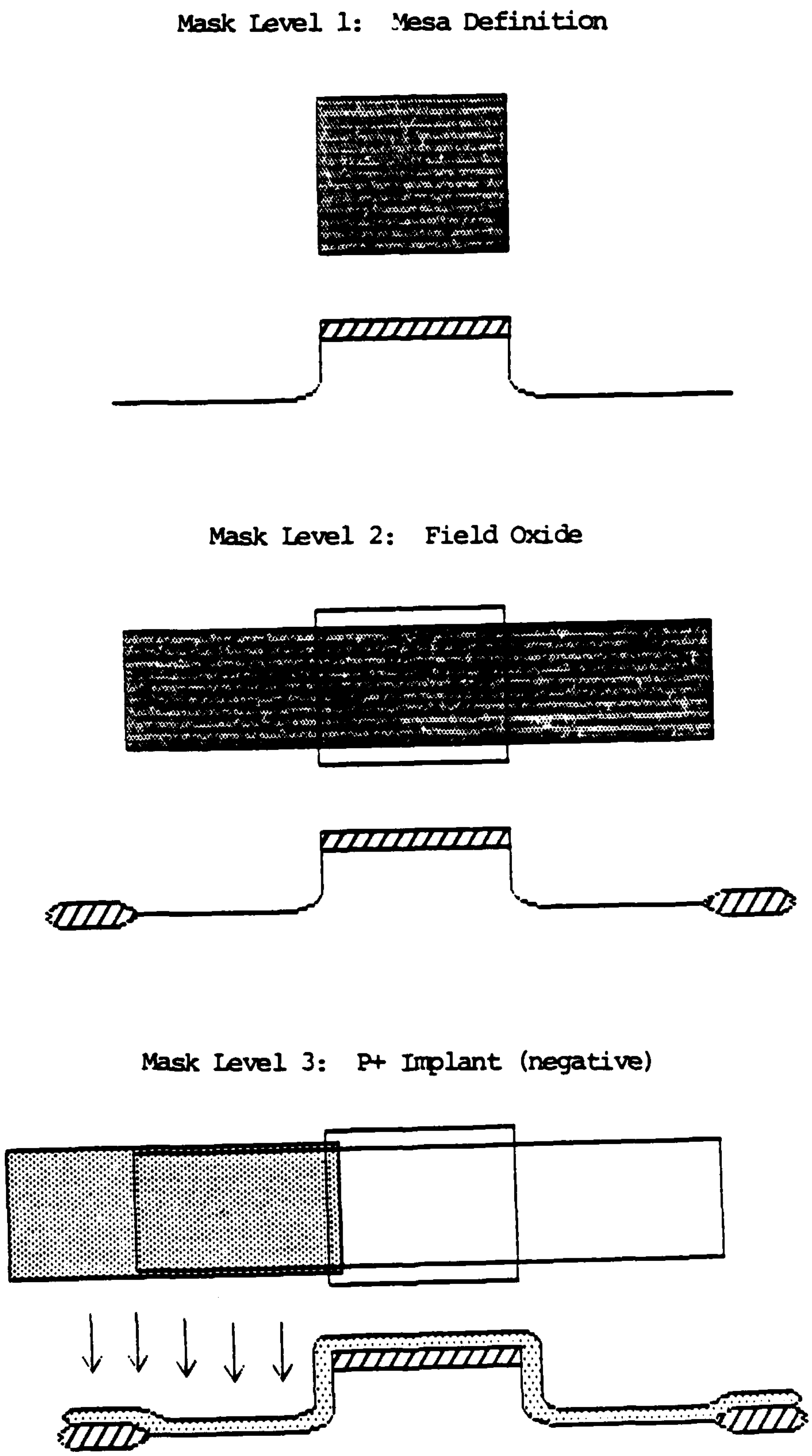
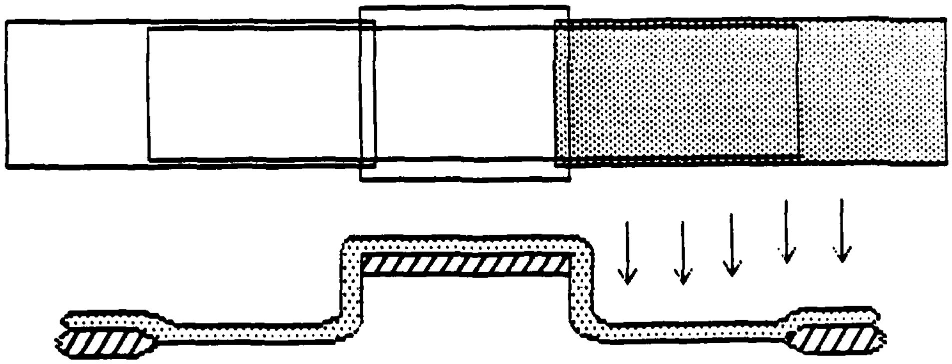
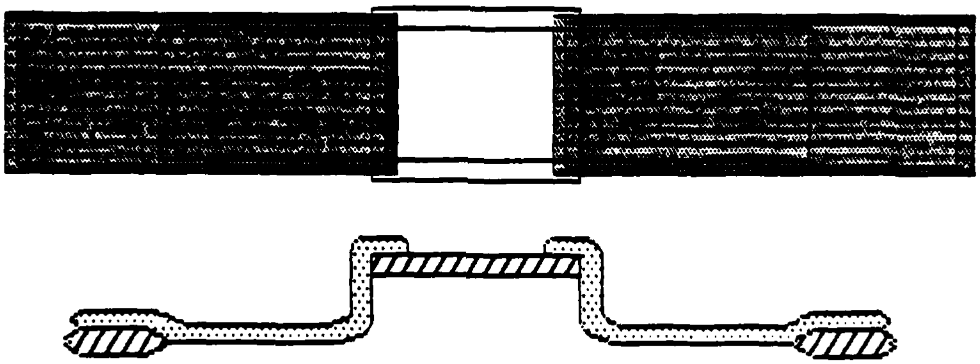


Figure 4.3: Mask Levels of PIN Diode Test Structure
(1 of 2)

Mask Level 4: N+ Implant (negative)



Mask Level 5: Poly Definition



Mask Level 6: Aluminim Pattern

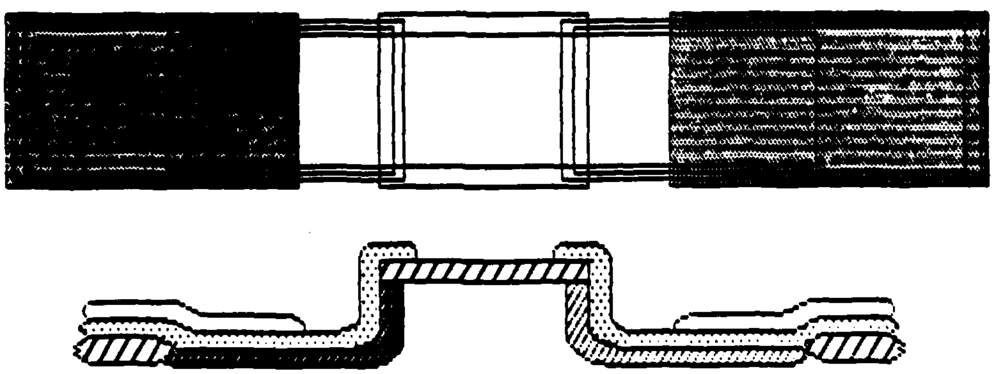


Figure 4.3: Mask Levels of PIN Diode Test Structure
(2 of 2)

μm up to 600μm in 150-μm steps. The purpose of these devices is to provide information on the effects of the side surfaces. The recrystallized material is expected to have directional properties depending on the scan direction of the electron beam. Because of this, several devices were rotated 90 degrees to measure the directional effect of the expected subboundaries.

The bottom of each die was reserved for test structures including the wide and rotated diodes described previously. There are two cross structures for measuring contact resistance from the aluminum to p-doped and n-doped polysilicon. Also included are two bridge resistors of p and n polysilicon with enough contacts to allow simple bar resistivity, van der Pauw resistivity, and Hall mobility measurements. Another important structure consists of long parallel mesa lines which are conformally covered with perpendicular p and n polysilicon lines to allow verification of the continuity of the polysilicon over the mesa steps. Finally, in the lower right-hand corner there is a section which is used during processing to evaluate key steps. It is basically a grating of long mesa lines of varying widths. After the initial deep silicon etch, for example, a sample can be cleaved across these lines and examined with a scanning electron microscope. After the LPCVD silicon nitride and polysilicon deposition, it is possible to see the conformity over this grating for both cases by using the SEM. Other test structures such as MOS capacitors or FETs were considered for the mask design, but they were not compatible with the process and were not included. The most useful electrical characterization information comes from the PIN diodes themselves.

4.3 Processing and Fabrication

In this section, a detailed explanation of the key processes necessary for the mesa PIN diode structure is presented. Among the many steps involved

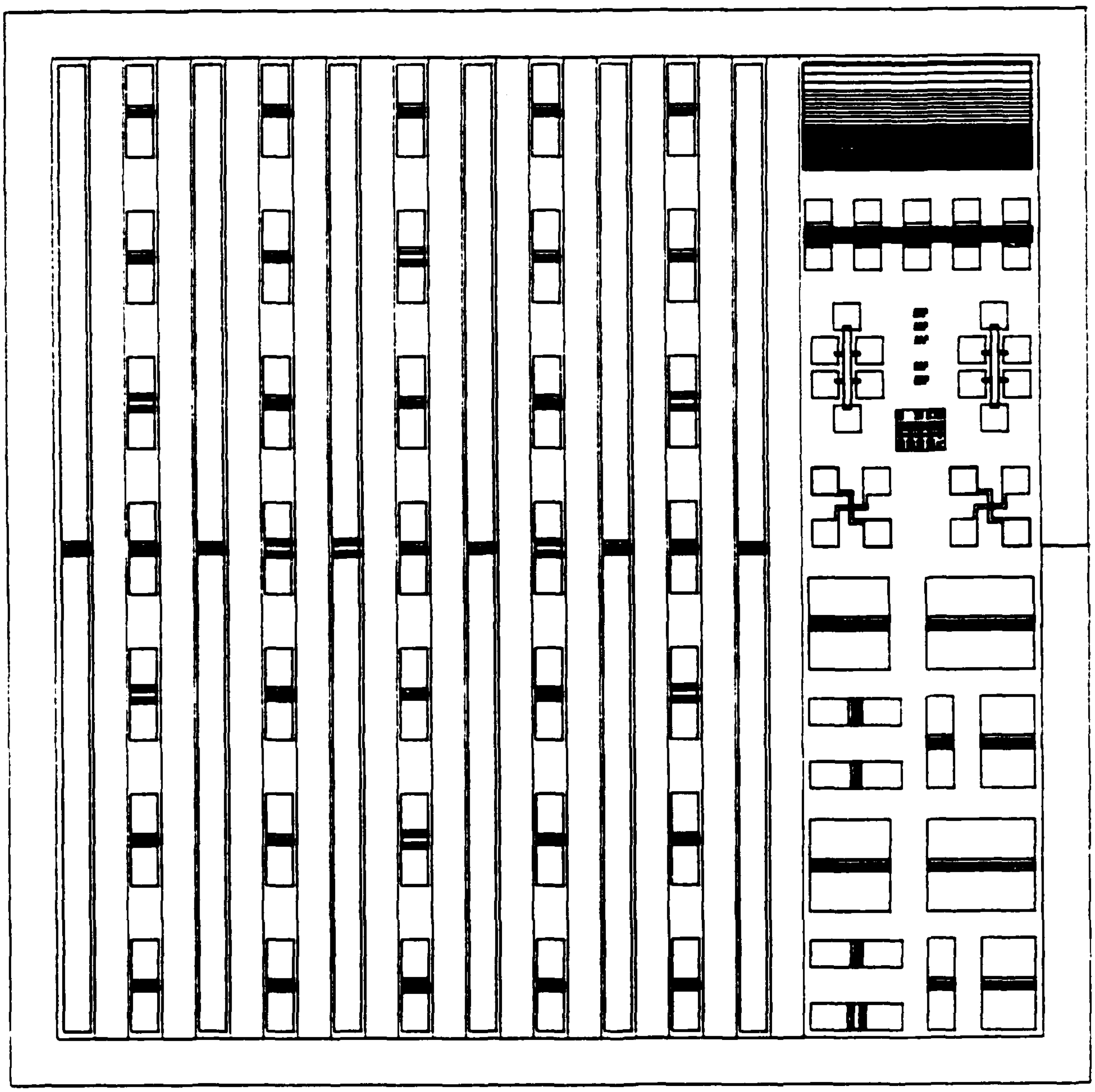


Figure 4.4: Overview of PIN Diode Mask

in the fabrication, two are particularly important and somewhat unique, namely the doped polysilicon diffusion source and the silicon trench etch for mesa formation.

Given the desired anisotropic profile of the reactive ion etch, it was necessary to develop a scheme whereby the donor and acceptor impurities could be introduced into the intended n and p sidewalls respectively. In addition, a method of making a good ohmic contact to the device is needed. The nearly vertical sidewalls of the mesa would not allow ion implantation into the critical end regions of the diode unless the sample was precisely angled during implantation. Also, it would be impossible for an evaporated metal film to conformally cover the end regions for a reliable, low-resistance contact.

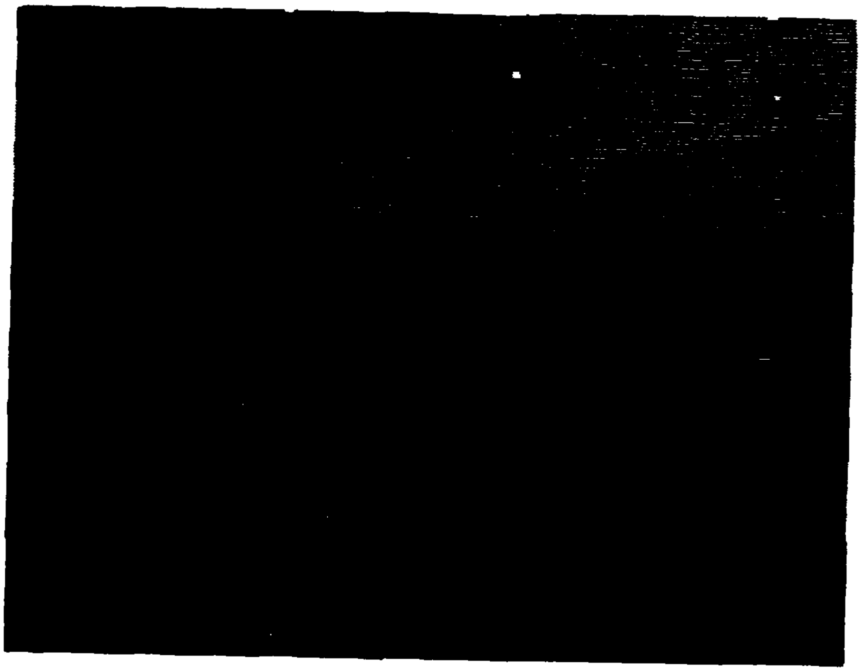
The concept of using ion-implanted polysilicon as a diffusion source solves these problems. The polysilicon can be deposited in a LPCVD system which provides a very uniform film that is conformal to the surface of the sample. This desirable conformal coating results from a deposition which is surface-reaction-rate limited. The results achieved are shown in Fig. 4.5, and 4.6. SEM photographs of the LPCVD polysilicon from the test-structure area of the chip, at 20Kx and 10Kx respectively. The problems of damage associated with ion implantation in crystalline material are not of concern for the polysilicon.

Another key point concerning this process results from the diffusion constants of dopants in polycrystalline silicon being much greater than in single crystal silicon. During the post-implantation drive-in, the implanted dopants redistribute in the polysilicon before any significant diffusion occurs into the substrate material. Thus, the polysilicon covering the sidewalls which were not directly implanted or which received only a fraction of the implant dose become doped by diffusion from any contiguous implanted section. This polysilicon "handle" process was used by Robinson et al.[23] for a unique joint-gate CMOS technology.

By continuing the high temperature drive-in with the diffusion source now effectively covering the mesa sidewalls, the p and n regions of the diode will be formed. After drive-in and subsequent delineation of the p^+ and n^+ diffused regions with a doping-dependent etch. Aluminum can now be evaporated onto the sample and patterned such that contact is made to the device through the polysilicon "handles." As noted earlier, the resistivity of doped polysilicon is appreciable so the metal must be close to the mesa edges to avoid parasitic resistances. Figure 4.7 is a SEM photograph of a cross-section of a complete 24µm I-region device.

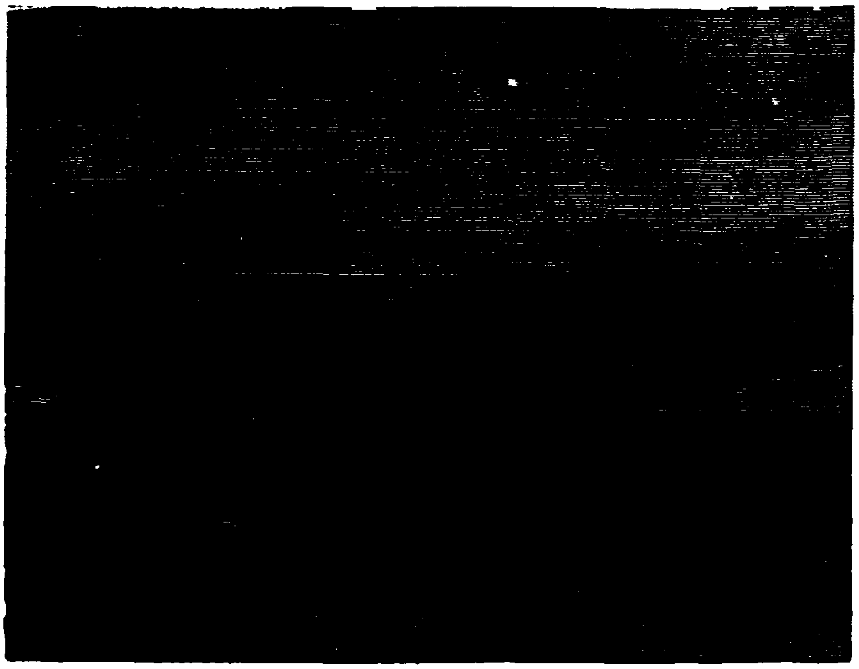
The deep silicon etch, which is necessary for improving the performance of the lateral PIN diode, can be accomplished in several ways. The first and simplest method is to use a standard silicon chemical etch solution of perhaps hydrofluoric and nitric acid. This, however, will result in an isotropic profile with a lateral undercut of the mask on the same order as the depth. This cannot be tolerated for the PIN diodes since the I-region width needs to be closely controlled.

A second possibilit, is an orientation-dependent wet chemical etch such as potassium hydroxide, n-propanol and deionized water, which etches silicon about one hundred times faster in the [100] direction than in the [111] direction. With a (100)-oriented wafer and a properly oriented mask such that perpendicular lines on the mask are aligned with the (110) directions of the wafer, the etch will proceed rapidly downward until the (111) planes have been exposed, and subsequent etching in the lateral direction will be negligible. The key problem with an orientation-dependent etch is that the crystal orientation of recrystallized silicon is not guaranteed a priori. Therefore, we



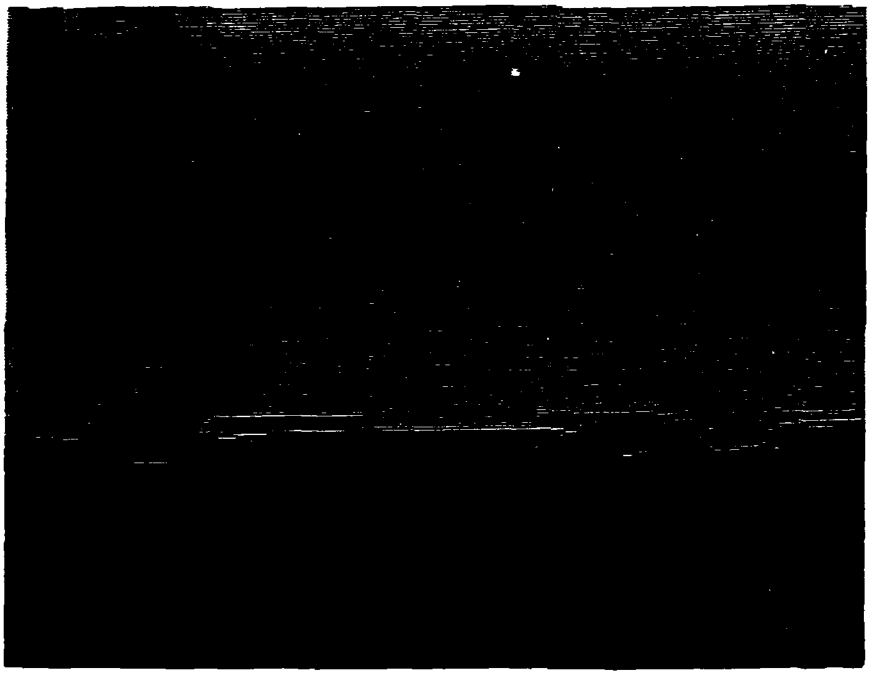
20Kx

Figure 4.5: Cross-Sectional SEM Photograph Depicting Conformal Coverage of Mesa by LPCVD Polysilicon Deposition



10Kx

Figure 4.6: Cross-Sectional SEM Photograph Depicting Conformal Coverage of Mesa by LPCVD Polysilicon Deposition



2.5Kx

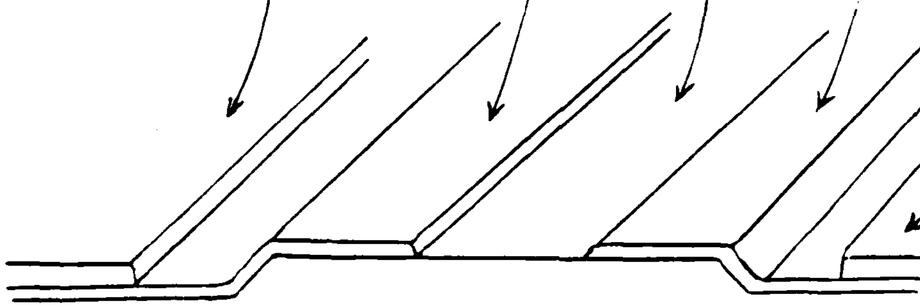


Figure 4.7: Cross Sectional View of Device after Fabrication

needed to develop a process which does not presuppose any particular orientation.

Reactive ion etching is capable of highly directional etching which is relatively independent of crystal orientation, so most of our efforts were directed towards developing a reliable reactive ion etching process. Since the equipment available to us was not protected against the corrosive properties of chlorine, we were limited to fluorine-based compounds such as CF_4, CHF_3, SF_6, and $CBrF_3$.

The difficulty with most of these gases is that the plasmas formed contain uncharged free fluorine radicals. This tends to cause isotropic etching and, therefore, undercutting of the mask. This problem is especially true of SF_6 where the high fluorine content per molecule results in high etch rates but almost no directionality. However, Matsuo(24) has reported that reactive ion etching of silicon with $CBrF_3$ can be accomplished with almost no undercut. It is hypothesized that the presence of bromine increases the silicon etch rate and/or decreases the silicon dioxide etch rate by possibly forming a protective buffer layer.

One of the main problems with reactive ion etching is the limited selectivity which can be achieved. The published results for $CBrF_3$ indicated that under the correct conditions, a selectivity of 8:1 between silicon and silicon dioxide was possible, but we were unable to reproduce this selectivity in our experiments. We expect that the selectivity is sensitive to various experimental parameters such as chamber pressure, gas-flow rates, and RF power. The best results obtained for the $CBrF_3$ reactive ion etch were a selectivity of 2:1 and an etch depth of approximately 2 μm as shown in Fig. 4.7.

Because of the limitations of silicon dioxide as the mask material, we investigated possible alternatives to be used in a two-layer mask configuration. Aluminum forms non-volatile compounds with fluorine and, thus, has a very low etch rate in fluorine-based plasmas. Therefore, evaporating a thin layer of aluminum on top of the silicon dioxide seemed to be the solution. This did not work as well as expected since a non-volatile compound, perhaps containing bromine, was apparently sputtered over the surface of the sample, and this retarded the etch rate. Also, the aluminum layer proved most difficult to remove.

Another alternative which was considered is based upon a different etchant gas, NF_3. Nitrogen trifluoride has the advantages of high etch rates, good selectivity between silicon and silicon dioxide, and no problems with carbon contamination. However, it was not readily available for our use and, since it is toxic, a vented gas cabinet along with additional plumbing would have been required. Because of both safety and time constraints, NF_3 could not be experimentally investigated during this program.

Because of the limited results from the more-attractive reactive ion etching experiments, a wet chemical-orientation dependent etch was selected for actual wafer processing. Since single-crystal (100) wafers have been chosen to evaluate the mesa structure with doped polysilicon "handles", the selectivity of the potassium hydroxide etch solution was sufficient. The samples were etched to a depth of 5 μm with only a slight loss in mask definition.

At the second photolithography step (see Fig. 4.3), we discovered that photoresist AZ1470 was inadequate for applications requiring step coverage greater than a few microns. The solution to this problem requires a higher viscosity photoresist which results in a much thicker coating for a given spin speed. This introduces some loss of resolution, but for our relatively large structures the effect is minor. Although such a resist (Shipley S1650 with a viscosity ~200 cSt) was ordered, delivery time was indefinite so wafers with a mesa height of only 2 μm were fabricated. The AZ1470 resist covered this step sufficiently, so the processing continued following the procedures obtained in Section 4.2. Upon receipt of the S1650, we found that it would work for the 5-μm mesa height. However, we emphasized the processing for the 2-μm mesa wafers due to the extensive delay. These device results are presented in the following section.

4.4 Device Results

In this section, we present results with the finished devices fabricated using single-crystal p-type 10 ohm-cm silicon wafers. The desired characteristics for a PIN diode are low on-state forward bias resistance, high reverse breakdown voltage and a constant capacitance beyond punch-through. The key parameter for demonstrating the quality of the diode is the resistance dependence upon DC forward-bias current as measured at microwave frequencies. Low values of resistance showing an inverse relationship with bias current would indicate conductivity modulation of the I-region through double injection. The measured values also would provide information on the lifetime of carriers in the I-region.

Much useful information can also be obtained through various DC and low-frequency (e.g. 1 MHz) measurements. From the diode I-V characteristic, we can find the reverse leakage current, the reverse breakdown voltage, the ideality factor, and speculate on the conduction mechanism. In addition, various high-level injection phenomena, such as Auger recombination and carrier-carrier scattering, can be observed. The C-V characteristic can provide the punch through voltage and the mid-region doping level.

In addition, information can be learned from the test section which was included on each chip. The resistance from the probe pads to the actual device can be estimated by first measuring the polysilicon bar resistors and the contract-resistance test structures. The doped polysilicon lines draped across several mesa steps provides an additional point for comparison besides testing for step coverage. Finally, the devices of constant I-region thickness but varying widths will help discern whether or not an observed phenomena is dependent on area and thus aid in formulating an explanation.

We initially present data obtained for the nominal 12 μm I-region diode having a width of 150 μm. Figure 4.8 shows the forward I-V characteristic of the device and indicates attractive rectification characteristics similar to a typical silicon pn junction diode. More information can be obtained from a plot of the log of the forward current versus voltage (Fig. 4.9). Note that there appears to be a region from 0.5 to 0.8 volts where the ideality factor is approximately two. This normally corresponds to high-level injection in a pn junction or double injection for the case of a PIN diode. Note also that there is no region where the ideality factor is one, a factor which is associated with the standard diffusion current model.

At low values of forward bias, the effects of generation and recombination in the space charge region are commonly the dominant mechanism, and these result in an ideality factor of two. Again referring to Fig. 4.9, below 0.4 volts the ideality factor is somewhat greater than two, which suggests that another conduction mechanism, most likely surface leakage, is significant.

Near 1.0 volt, the slope of the log of the current versus voltage begins to decrease. This can be explained by various mechanisms. Under conditions of high-level injection, mobile carriers interact with one another in a process known as carrier-carrier scattering resulting in a reduction of ambipolar

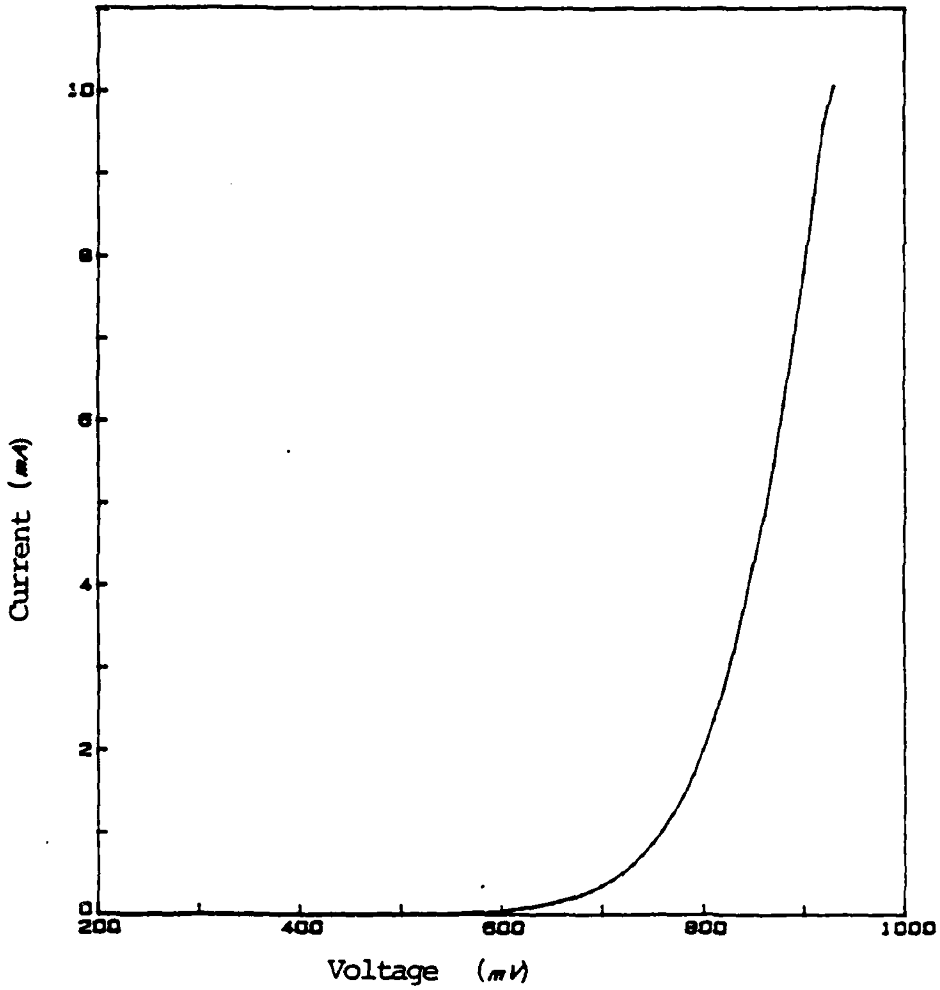


Figure 4.8: Forward I-V Characteristic of 12 μm
I - Region, Standard Width PIN Diode

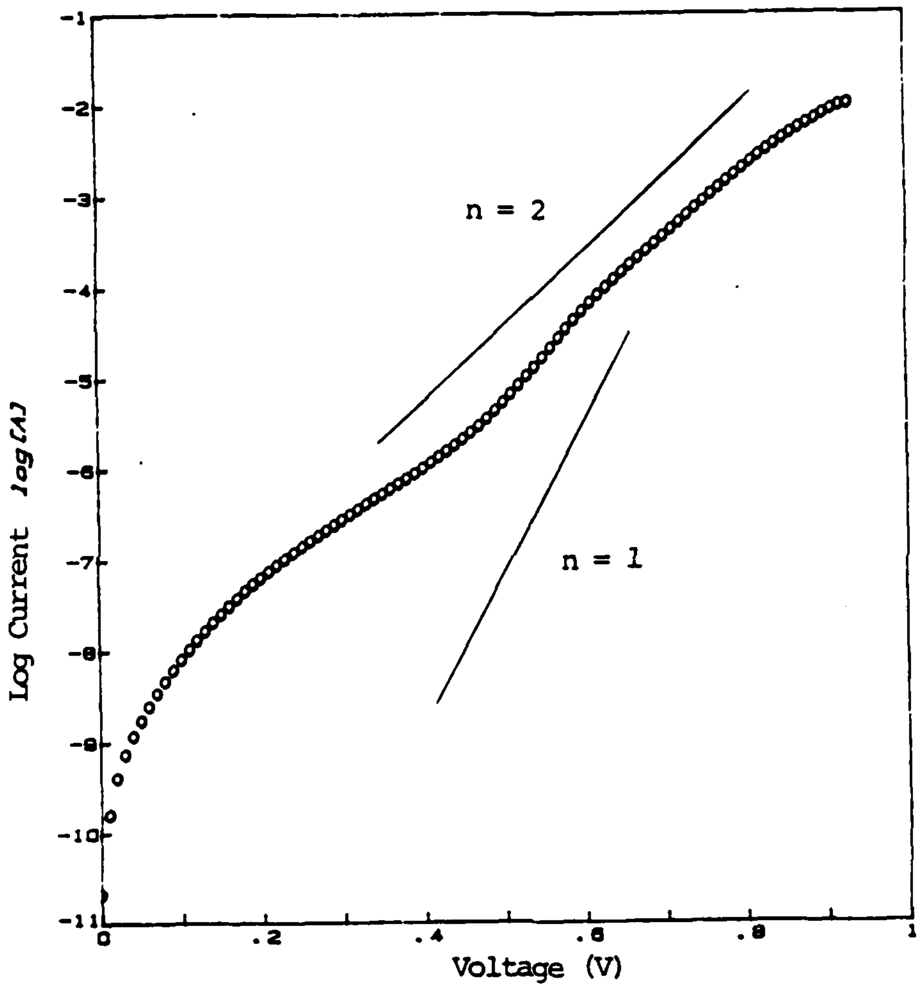


Figure 4.9: Forward Log I vs. V Characteristics of
12 μm I - Region, Standard Width PIN Diode

mobility and, hence, current. A second effect which can be observed under high-level injection conditions is Auger recombination in which direct recombination is possible in an indirect semiconductor such as silicon with the help of an additional carrier. This process serves to reduce the lifetime of carriers in the I-region. Finally, at very high current levels, the parasitic series resistance becomes the limiting factor. The I-V characteristic was measured up to currents of 200mA, and these measurements indicated a maximum series resistance of approximately 3 ohms. This is much smaller than the 13 ohms which is determined from the upper end of Fig. 4.9, so the decrease in slope at around 0.9 volts appears to be dominated by carrier-carrier scattering or Auger recombination.

Figure 4.10 is a plot of log I versus V with an expanded voltage scale which includes the reverse bias conditions. The reverse leakage current is seen to be on the order of 100 nA. If the reverse bias is increased further, breakdown is observed at approximately 160 volts. This value corresponds to a critical field of about 3×10^5 volts/cm and is close to the expected value for the starting material doping concentration.

The C-V characteristic of the diode could not be accurately measured since the probes used contribute a parasitic capacitance of about 1 5 pF (which is greater than the minimum capacitance of the PIN diode by two orders of magnitude). We did not develop a shielded three terminal capacitance setup since information to be obtained did not warrant the investment.

In addition to the diode data, the doped polysilicon bar resistors measured 367 ohms and 287 ohms for p-type and n-type doping, respectively. This translates into a sheet resistance of 34.9 ohms/square for the boron-implanted polysilicon and 27.2 ohms/square for the phosphorus-implanted case. The lower

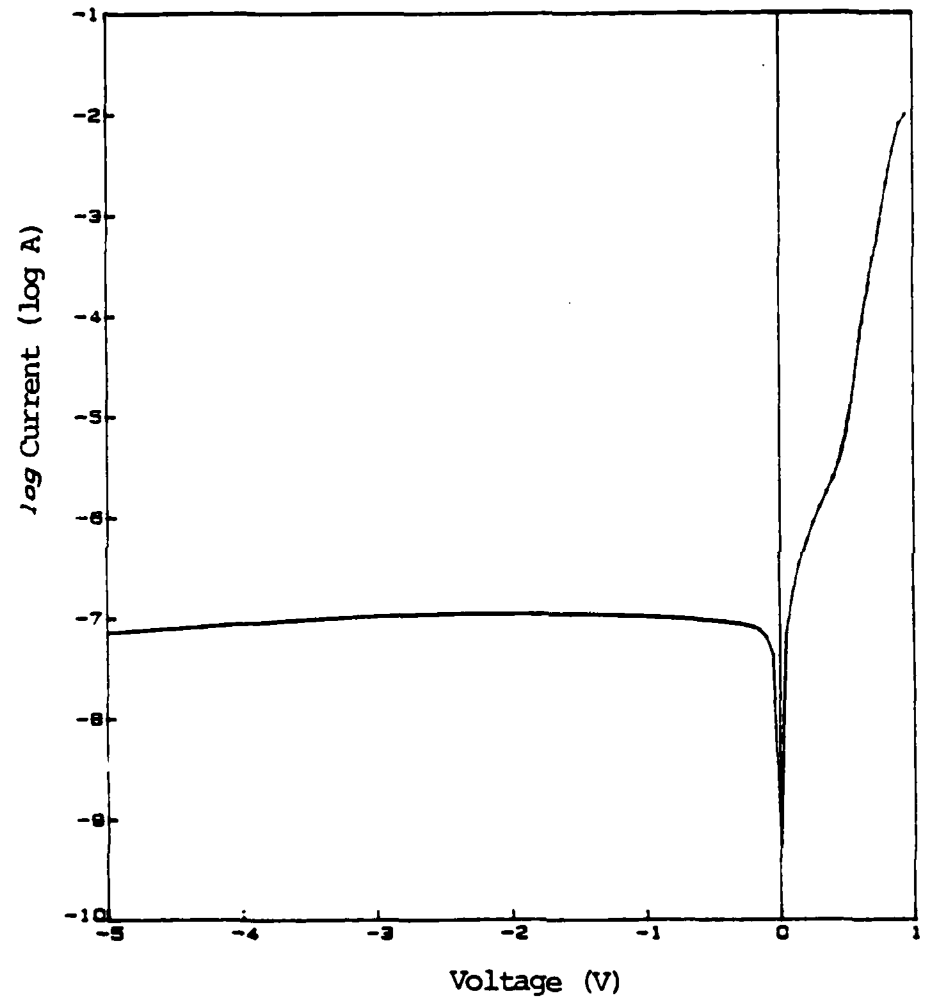


Figure 4.10: Expanded Log I vs. V Characteristic of
12 μm I - Region, Standard Width PIN Diode

n-type resistivity is expected since the mobility of electrons is somewhat higher than that of holes.

The doped polysilicon lines over mesa steps were measured and found to have resistances of 60.8 ohms and 47.6 ohms for p- and n-type doping, respectively. These relatively low values confirm the conformality of the LPCVD polysilicon process. Note that the resistance of the n-type structure is lower and the ratio between the resistances is almost exactly the same as for the bar resistors. By taking into account the geometry of these test structures and making use of the bar resistor data, approximate values of resistivity for the doped polysilicon itself over the mesa oxide can be calculated. The resistivity of the p-type polysilicon is 7×10^{-3} ohm-cm while the n-type is 5.5×10^{-3} ohm-cm, compatible with published results.(25)

The series resistance for the device can be estimated from the data above. The main contributions are the polysilicon resistance from the aluminum line edge to the base of the mesa and that covering the side wall. In retrospect, the aluminum-to-mesa separation, which was chosen to be 4 μm to allow for alignment error, was too conservative and adds unnecessary series resistance. The estimated value for a device width of 150 μm is 1.7 ohms. Allowing for an additional 0.6 ohm for the side-wall polysilicon, the estimated series resistance compares favorably with the 3.0 ohm value obtained from the I-V characteristic.

Considering the high current (~200 mA) regime for devices of varying I-region dimension (with constant width), the series resistance remains the same for the 6 μm and 24 μm diodes but is 50 percent larger for the 48 μm diode. This indicates that high-level injection effects have resulted in an ambipolar diffusion length of approximately 30 μm. In other words, the 48 μm device is effectively a "long" diode.

When devices with a constant 12 μm I-region dimension but varying widths are compared, the results are somewhat unexpected. The parasitic series resistances should be inversely dependent upon device width. Instead, we measured 2.5, 2.35, and 2.2 ohms for the 300 μm, 450 μm and 600 μm devices respectively, compared to 3.0 ohms for the 150 μm device. However, the diodes are not completely in their series-resistance limited domains at a current of 200 mA, and high-level injection effects (carrier-carrier scattering and Auger recombination) are not easily scaled.

For the different I-region dimensions, the forward current below 0.4 volts was investigated. Bulk mechanisms like single-carrier injection and generation-recombination current are not in agreement with the observed voltage dependence. This current is attributed to surface leakage at the interface between the mesa oxide and the oxide covering the ends of the device. Figure 4.11 shows two forward log I vs. V characteristics for the same device but from different parts of the wafer. The only difference is the leakage current, which is most likely a result of the nonuniformity of the polysilicon plasma etching process.

High reverse biases were applied to the standard 150 μm wide diodes to determine their breakdown voltages. The results are 80V, 150V, 200V and 250V for I-layer dimensions of 6 μm, 12 μm, 24 μm and 48 μm, respectively. The two larger diodes break down at a voltage which is lower than expected. Each displays a soft knee around 175 volts which may indicate a possible surface breakdown mechanism.

Returning to the regions of the forward log I versus V characteristics where high level injection and possibly diffusion-limited current flow are occurring, the various combinations of I-region dimension and device width all exhibit two regions of constant slope from 0.5 to 0.6 volts and from 0.6 to

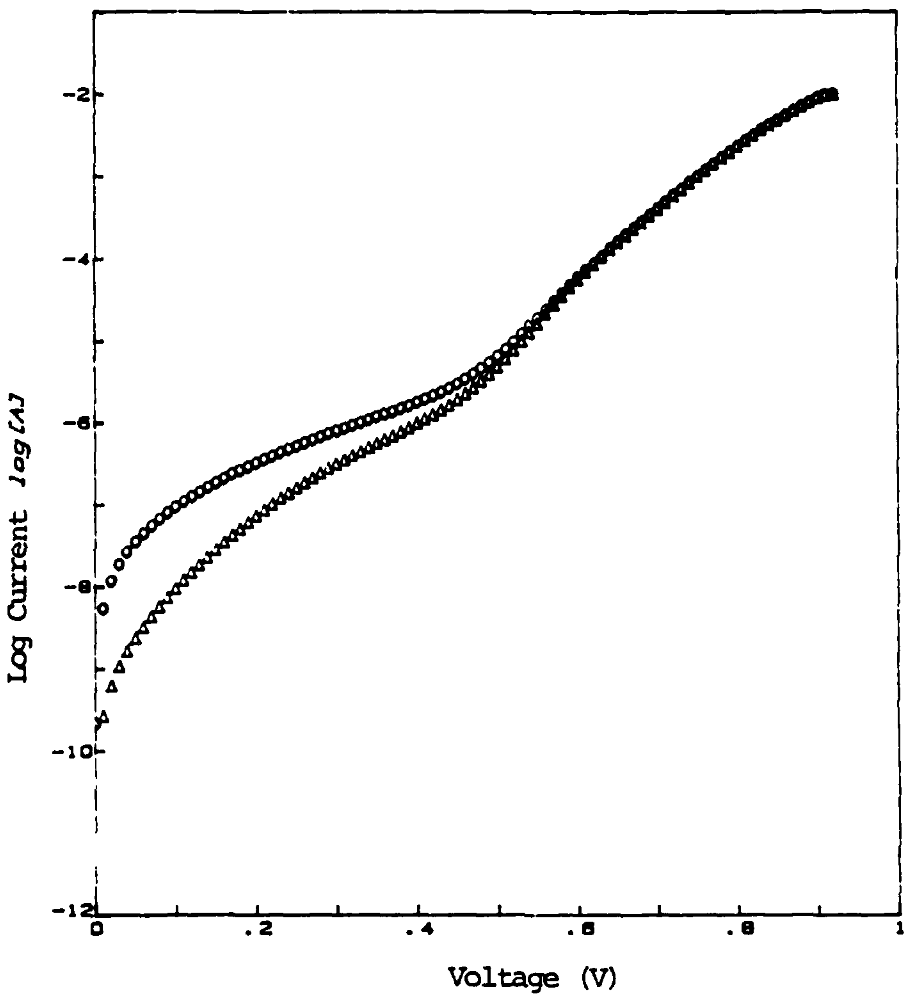


Figure 4.11: Forward Log I vs. V Characteristic For Two 6 µm I - Region, Standard Width PIN Diodes From Different Parts of Reference Wafer

0.8 or 0.9 volts. The second region is extended before a decreasing rate of current increase occurs for the wider devices since the current density is correspondingly lower. Also the slope in this region drops for a longer I-region dimension giving a higher ideality factor. This is likely caused by the added effects of surface recombination.

At the time this report was written, the wafer from which most of these results were obtained were just diced into individual chips. This is necessary for the testing of the diodes at microwave frequencies since each chip must be mounted individually onto a specially prepared fixture. The mask set included six microwave-testable devices on each die, with aluminum contact pads extending to the edge of the chip to allow for easier RF mounting.

The test fixture is basically composed of two 50-ohm microstrip gold-on-alumina lines separated by a distance slightly shorter than the chip width. The chips will then be flip-mounted with indium performs providing the contact between the aluminum and the gold to allow for easy removal and remounting. The 50-ohm lines are directly bonded to two OSM connectors, one of which will be terminated with a 50-ohm load. The other end will be connected to a signal generator and measurement apparatus. Extensive RF testing and evaluation could not be completed prior to submission of this report, but initial results demonstrating conductivity modulation of RF signals are presented in Appendix D.

5. EVALUATION OF CURRENT STATUS AND FUTURE DIRECTIONS

In this section, we summarize the current status of the two major components of our research program, specifically the silicon-on-alumina recrystallization experiments and the development of surface-oriented PIN diodes. In addition, we describe near-future directions of this innovative and promising approach for achieving cost effective, high-performance microwave monolithic control components.

5.1 Silicon-on-Alumina Recrystallization Experiments

The development of high-quality, single-crystal silicon-on-alumina films would be a straightforward extension of past work concerning the recrystallization of thin silicon films over oxidized-silicon substrates if not for two major limiting factors. One factor is the surface quality of the alumina substrate; a smooth surface is required in order to support useful films. The other factor is the mismatch between the thermophysical properties of alumina and silicon; if uncompensated, a large mismatch can lead to destructive stress levels. Both factors have significant impact on the quality of recrystallization films.

An alumina substrate cannot be polished to the same degree as a conventional silicon wafer. The highest-grade alumina substrates which are commercially available have surface roughness of about 0.01 μm, which also suffer from grain pullouts as fired substrate have fewer grain pullouts but an intolerable roughness of about 0.10 μm. In order to obtain a smooth surface to support a thin silicon film for recrystallization, we have used a buffer layer of silicon dioxide. If the glass layer is phosphorus doped, a reflow after deposition can further improve surface planarity. In future work, it may be desirable to develop a more complicated planarization process, perhaps one which employs plasma etching in conjunction with a spin-in organic planarization layer.

Apart from the surface planarization problem, it is probable that the glass buffer layer will still be required in order to alleviate stress in any subsequently-deposited thin films. As noted in Section 2.3.3, the coefficient of expansion of alumina is greater than that for silicon. In the absence of a buffer layer for stress relief, the silicon film experiences tensile stress while being heated prior to recrystallization, the stress is relieved once the silicon film has melted, and the recrystallized silicon film undergoes compressive stress while cooling. The tensile and compressive stresses can lead to cracking and blistering failure, respectively. Moreover, the tensile stress can exacerbate non-uniform zone melting.

Fortunately, the silicon dioxide buffer layer can be made thin (1-10 μm) so its presence should not adversely affect RF performance in MMIC applications. Phosphorus doping, for reduced glass viscosity at high temperatures, is not a serious problem when lateral PIN diode designs are used (see Chapter 4).

At the beginning of our program, we stressed the development of an electron-beam as the heat source for zone-melting recrystallization experiments because we believed that it would allow better control of the molten zone. An electron-beam apparatus has shown promise in experiments concerning the recrystallization of silicon over oxidized silicon substrates at other laboratories. However, for the case of silicon-on-alumina recrystallization experiments performed with our electron-beam system, the thermal stresses which are induced during an inherently non-uniform heating process tend to cause sample breakage and these stresses have been difficult to overcome with the substrate heating obtained. This problem has not been as severe in our experiments which employed a graphite strip heater. It might be possible to develop an improved electron-beam recrystallization apparatus in which thermal gradients are reduced by virtue of an increased substrate temperature. However, our recent results with a graphite strip heater have been encouraging and we expect to use a graphite strip heater for experiments in the near future (island recrystallization advantages of electron-beam discussed in Appendix C).

We believe that our understanding of materials problems which are related to zone-melting recrystallization of silicon-on-alumina films is such that future experiments can be more directly tied to device-related issues. Of particular concern is carrier lifetime and its relationship to subboundary control. We expect that the issue of recrystallization control over large areas will become a major problem as this work progresses.

5.2 Surface-Oriented PIN Diodes

Although microwave PIN diode technology has been well developed previously, the focus has been dominated by discrete vertically-oriented structures. Because of the constraints of the recrystallized-silicon film and the monolithic circuit implementations, lateral PIN diode structure is quite unconventional and innovative. In particular the use of the doped polysilicon "handles" and deep mesa structure has resulted in a promising alternative for a hybrid-based technology using single-crystal silicon (as well as meeting our primary objective of compatibility with recrystallized silicon films on alumina).

In developing this technology base we started with 10 ohm-cm silicon, rather than 1000 ohm-cm material useful for microwave PIN diodes. After complete evaluation of the devices described in Chapter 4, resistivity requirements for recrystallized material can be obtained, as reduced resistivity needs are more compatible with recrystallization technology. RF resistance measurements confirm (see Appendix D) the DC I-V data indication that double-injection has been achieved under forward bias with tolerable series resistance. The large breakdown voltages (150 to 200 V) obtained indicate that any surface leakage is not critical for microwave applications. Two difficulties limit the performance of the presence devices. First, the use of a 2-μm rather than a 5-μm mesa when combined with our nominal 150-μm width results in a small cross sectional area. When combined with the 10 ohm-cm material, our forward DC current range for double injection is limited. This limited range results in difficulty in confirming PIN diode quality without more precise RF measurements. The second difficulty is the conservative overlay metal (aluminum)-to-mesa edge in the mask design. This 4-μm spacing results in a significant series results (approximately 2 ohms) with a 150 μm width and limits the achievable RF resistance obtained by conductivity modulation of the I layer. Fortunately both these difficulties are easily overcome in a second-iteration design.

In summary, our lateral PIN approach using a deep mesa and doped polysilicon handles has proven to be an attractive approach to monolithic PIN diode fabrication. Additional RF characterization of the fabricated PIN diodes is necessary for full evaluation, but any foreseeable problems could be overcome in the next design iteration.

5.3 Research Publications

While our research results are not yet complete, we anticipate the following means of disseminating our research results:

- A paper on the recrystallization results reported in Chapter 3 has been accepted for presentation at the November '87 Materials Research Symposium in Boston (and we expect publication in the related referred conference proceedings).

- A publication in Applied Physics Letters is planned based upon the results of the stress analysis of Chapter 2, the results of Chapter 3 and an additionally planned experiment using variably sized recrystallization grids.
- A publication is planned on the lateral PIN diode structure using doped polysilicon "handles" and deep mesas based upon the low RF resistance achieved in the microwave testing (see Appendix D).

While we did not achieve the fabrication of PIN diodes on recrystallized films of silicon-on-alumina during the second year of the program, significant advances have been made in three key areas of the program, namely, experimental realization of recrystallized silicon-on-alumina films over 1 inch square substrates; analysis of the effects of stress on recrystallized film quality to provide guidance for the experimental program and evaluation of the long-range potential of the technology; and demonstration of a PIN diode structure compatible with recrystallized silicon films on alumina, monolithic implementation of microwave circuitry and good-quality PIN diode performance.

References

1. E.W. Maby and R.J. Gutmann, Si-on-Alumina Phase Shifters, RADC-TR-86-136, Oct. 1986.
2. A. Gat and J.F. Gibbons, Appl. Phys. Lett. 32, 142 (1978).
3. T.J. Stultz and J.F. Gibbons, Appl. Phys. Lett. 39, 498 (1981).
4. E.W. Maby, M.W. Geis, Y.L. LeCoz, D.J. Silversmith, R.W. Mountain and D.A. Antoniadis, IEEE Electron Device Lett. EDL-2, 241 (1981).
5. M.W. Geis, H.I. Smith, B-Y Tsaur, J.C.C. Fan, E.W. Maby and D.A. Antoniadis, Appl. Phys. Lett. 40, 158 (1982).
6. J.A. Knapp and S.T. Picraux, J. Appl. Phys. 53, 1492 (1982).
7. D.B. Rensch and J.Y. Chen, IEEE Electron Device Lett. EDL-5, 38 (1984).
8. B-Y Tsaur, M.W. Geis, J.C.C. Fan, D.J. Silversmith and R.W. Mountain, Appl. Phys. Lett. 39, 909 (1981).
9. B-Y Tsaur, J.C.C. Fan, R.L. Chapman, M.W. Geis, D.J. Silversmith and R.W. Mountain, IEEE Electron Device Lett. EDL-3, 398 (1982).
10. E.W. Maby and D.A. Antoniadis, Appl. Phys. Lett. 40, 691 (1982).
11. E.W. Maby, H.A. Atwater, A.L. Keigler and N.M. Johnson, Appl. Phys. Lett. 43, 482 (1983).
12. J.C.C. Fan, B-Y Tsaur, R.L. Chapman and M.W. Geis, Appl. Phys. Lett. 41, 186 (1982).
13. B-Y Tsaur, J.C.C. Fan and M.W. Geis, Appl. Phys. Lett. 41, 83 (1982).
14. H.A. Atwater, H.I. Smith and M.W. Geis, Appl. Phys. Lett. 41, 747 (1982).
15. B-Y Tsaur, J.C.C. Fan and M.W. Geis, Appl. Phys. Lett. 40, 322 (1982).
16. B-Y Tsaur, H.K. Choi, C.K. Chen, R.W. Mountain and J.C.C. Fan, IEDM Tech. Digest, p. 812 (1984).

17. M.W. Geis, H.I. Smith, B-Y Tsaur, J.C.C. Fan, D.J. Silversmith and R.W. Mountain, J. Electrochemical Soc. 129, 2813 (1982).

18. Z.A. Weinberg, V.R. Deline, T.O. Sedgwick, S.A. Cohen, C.C.F. Aliotta, G.J. Clark and W.A. Lanford, Appl. Phys. Lett. 43, 1105 (1983).

19. H.W. Lam, R.F. Pinizzotto, S.D.S. Malhi and B.L. Vaandrager, Appl. Phys. Lett. 41, 1083 (1982).

20. L. Pfeiffer, T. Kovacs and K.W. West, Appl. Phys. Lett. 47, 157 (1985).

21. B. Battershall and S. Emmons, IEEE Trans. Electron Devices, ED-15, 507 (1968).

22. J.C. Sturm, J.P. McVittie, J.F. Gibbons and L. Pfeiffer, IEEE Electron Device Letters, EDL-8, 104 (1987).

23. A.L. Robinson, D.A. Antoniadis and E.W. Maby, IEDM 83, 530 (1983).

24. S. Matsuo, Appl. Phys. Lett., 36, 768 (1980).

25. M.M. Mandurah and K.C. Saraswat, J. Electrochemical Soc., 126, 1019 (1979).

Appendix A: Abstract, Table of Contents, and Plans for Second Year from First Annual Report

ABSTRACT (ANNUAL REPORT I)

This research program is aimed toward a microwave monolithic integrated circuit (MMIC) technology using recrystallized silicon-on-insulator substrates. Such a technology would permit PIN diode phase shifters to be fabricated with higher power-handling capability and lower insertion loss than conventional MMIC control circuits using GaAs MESFETs. Moreover, at frequencies below 10 GHz, where substrate area requirements can be extensive, the silicon-on-insulator substrate technology can be less expensive. This research program stresses silicon-on-alumina recrystallized films, followed by growth of silicon epitaxial layers and *surface-oriented* PIN diode fabrication.

In the first year of the program we have accomplished the following:

1. initial recrystallization of sputtered silicon on alumina with a CVD SiO_2/sputtered Si_3N_4 encapsulation layer and an evaluation of recrystallization difficulties.

2. modification of an electron-beam system to permit controlled recrystallization experiments.

3. a design tradeoff of surface-oriented PIN diodes versus vertical devices for MMIC applications.

4. evaluation of microwave-detected photoconductivity decay as a measurement technique for thin-silicon-film recombination lifetime evaluation.

5. definition of a program plan for the second year.

The principal investigators acknowledge the capable assistance of Mr. Ted Letavic in executing many of the tasks of this program and the encouragement and support of the contract monitor, Dr. Eurig Davies.

Table of Contents (Annual Report I)

Appendices

Appendix A

Plans for Second Year (Annual Report I)

In this section we describe our research plans for the second contract year. As in the first contract year, we are dividing the work into two major efforts. The first concerns silicon-on-alumina recrystallization problems and sample preparation (Section A). The second concerns the general problem of PIN diode fabrication on silicon-on-insulator films (Section B).

A. Recrystallization Experiments and Characterization

Two problems related to silicon-on-alumina sample preparation need to be resolved. The first concerns the degree of surface irregularity (+/- 0.1 m minimum) which is inherent to the starting alumina substrates. We hope to alleviate this problem by one of several procedures (in order of desirability):

- o deposition of a phosphorus-rich glass and reflow prior to silicon deposition.
- o utilization of thicker silicon films.
- o development of a chemical- or plasma-etch planarization process.

Once a procedure has been established for depositing silicon films which are reasonably smooth, we shall have the encapsulation films prepared at another laboratory by means of a process which is known to work reliably for the case of silicon films over oxidized silicon substrates. We hope to eventually obtain an encapsulation layer deposition process for our own laboratory, but we believe that this is not of central importance to our program at this time. After sample preparation problems have been resolved, we intend to perform a variety of recrystallization experiments using the electron-beam system. Similar experiments will be performed with a graphite-strip-heater apparatus as controls. Samples which have good crystallographic texture and low defect densities will be used for PIN diode fabrication.

B. PIN Diode Fabrication and Characterization

After considering the advantages and disadvantages of the vertical and lateral structure, we have decided to emphasize the lateral structure during the next year, principally because of the compatibility with monolithic circuit fabrication, elimination of the large RF spreading resistance and potential separation of recrystallization defects and the active region of the device.

During the next quarter the lateral device mask will be finalized, including mostly discrete PINs but also a SPDT switch and test structures. While emphasizing recrystallization experiments, PIN diode aspects unique to the lateral structure will be investigated while the mask set is obtained externally.

After the mask set is received, PINs will be fabricated:

1. starting with high resistivity silicon wafers to debug our processing procedures and to permit the lateral geometry effects to be quantified.

2. starting with silicon recrystallized over SiO_2 (then layer over a S_i wafer) to obtain a baseline capability for conventionally recrystallized silicon.

3. starting with silicon recrystallized over alumina (after appropriate planarization as described in Section 6.1).

While the third series of PIN diodes is of direct interest in our research, we believe that the first two steps are necessary to provide an appropriate data base for evaluation of the potential of the SOI technology for monolithic PIN diode phase shifters.

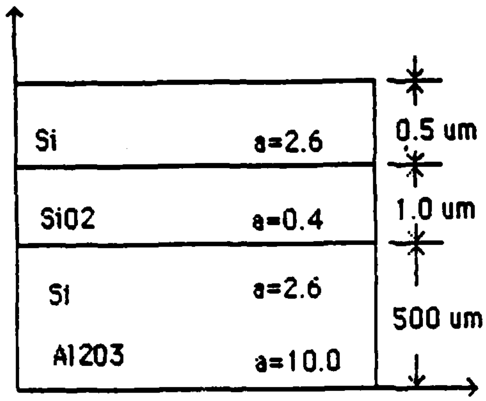
APPENDIX B

STRESS CALCULATIONS

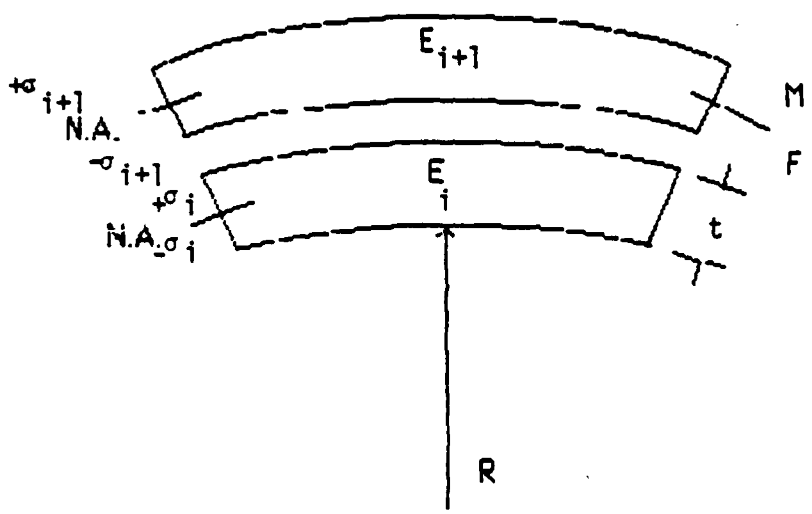
SOI COMPOSITE STRUCTURE

Silicon or Alumina substrate

a=linear coefficient of expansion



MATHEMATICAL MODEL FOR SOLUTION



where N.A = nuetral axis

R = bending radius

M = bending moment

F = induced force

t = film thickness

σ = stress at interface

The dominant strain contibutions within a SOI composite are differential thermal expansion (DTE) and pure bending. The solution technique for the stresses within the thin films involves the formation of a linear system of forces and moments due to the applied interfacial strains. The forces and moments within a given film are a result of the action of other films within the composite. All moments act through the nuetral axis of the film. Static equilibrium conditions apply at the thin film free surfaces.

For a three layer composite;

$\Sigma F = 0 \qquad F_1 + F_2 + F_3 = 0$ B.1

$\Sigma M = 0 \qquad M_1 + M_2 + M_3 + F_1({}^{t_1}/_2) + F_2(t_1 + {t_2}/_2) + F_3(t_1+t_2+{t_3}/_2)$ B.2

Pure Bending Moment; $M_i = \frac{E_i I_i}{R} = \frac{Et_i^3}{12R}$ B.3

Maximum Bending Strain; $\varepsilon = \pm \frac{t_i}{2R}$ (t = tension) B.4

Normalized DTE Strain; $\varepsilon_{ij} = (\delta_i - \delta_j)\,\Delta T$ B.5

A linear system of equations is obtained by evaluating the difference in total strain across the thin film interfaces.

Strain at top of ith layer; $\varepsilon_i = \frac{F_i}{E_i t_i} + \frac{t_i}{2R}$ B.6

Strain at bottom of i+1 layer; $\varepsilon_{i+1} = \frac{F_{i+1}}{E_{i+1}\, t_{i+1}} - \frac{t_{i+1}}{2R}$ B.7

Application of coherent boundary conditions for N layer composite yields

$$\Sigma\,[\epsilon_i - \epsilon_{i+1}] = \frac{F_{i+1}}{E_{i+1}\,t_{i+1}} - \frac{E_i}{E_i t_i} - \frac{(t_i + t_{i+1})}{2R} \qquad \text{B.8}$$

where $(\epsilon_i - \epsilon_{i+1})$ represents the total strain differential between the ith and the i+1 layers.

The linear system of (N-1) differential strains is coupled with the static equilibrium conditions (B.1, B.2) to solve for the N stresses and the bending radius R. These are sufficient to uniquely quantify the stress scenario within the thin films. If the Young's Modulus is assumed constant for the film composite the following results:

$$R = t^3[6(t_1 t_2 \epsilon_{12} + t_2 t_3 \epsilon_{23} + t_1 t_3 \epsilon_{13})]^{-1} \qquad \text{B.9}$$

$$\sigma_i = E_j\,[\sum_{i=1}^{N} (t_i \epsilon_{ij}/t + \frac{t_i k_i}{2R}) + (y - \frac{t_j}{2}) / 2R] \qquad \text{B.10}$$

where

$$K_i = \begin{cases} 1 & i<j \\ 0 & i=j \\ -1 & i>j \end{cases} \quad \text{and } t = \sum_i t_i$$

It is clear that the dominant term in the film stress equation B.10 is ($t_i \epsilon_{ij}/t$) which indicates that the substrate dominates the stress value within the thin surface films. Equations B.9 and B.10 where utilized for various SOI composite structures for stress evaluation. Residual stress due to temperature cycling during sequential film deposition was included, and the results appear in Figures 2.6 and 2.7 for comparison.

Appendix C

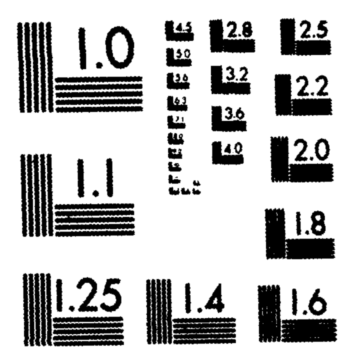
Comparison of Graphite Strip Heater and Raster-Scanned Electron Beam for Silicon-on-Alumina Films

In this research program, two different primary sources have been utilized for the creation of a molten zone in the polysilicon film; namely, a graphite strip heater and a raster-scanned, focused electron beam. The graphite strip heater is a non-coherent, radiative heat source, while the electron beam system is a biaxially focused, conductive heating system. The driving force for the development of a focused primary heat source (laser, electron beam) has been to reduce the total area of the molten silicon zone, hence reducing the surface forces exerted by the molten silicon on the capping structure. The reduction of these forces has been investigated as a means of avoiding agglomeration. The electron beam and the graphite strip heater have drastically different influences on the crystal growth mechanism during zone melt recrystallization. To compare the two heating sources, one must investigate the assumed mechanism for resulting texture, lateral intensity gradients, energy absorption mechanisms, and lateral thermal forces imposed upon the capping structure. These issues are presented in detail for each heating system, and the relative advantages and disadvantages of each system are presented.

The graphite strip heater system consists of a thin, resistively heated graphite rod which is suspended above an SOI sample. During a typical graphite heater zone melt recrystallization experiment, the upper strip power is increased slowly until partial meltig of the polysilicon is observed. As the polysilicon makes the phase transformation to the partially melted state, there is a significant change in the optical properties of the film. The reflectivity increases upon melting, which results in a reduction of absorbed

AD-A193 359 SILICON-ON-INSULATOR PIN DIODES(U) RENSSELAER POLYTECHNIC INST TROY NY DEPT OF ELECTRICAL COMPUTER AND SYSTEMS E NGINEERING E W MABY ET AL. DEC 87 2/2

UNCLASSIFIED RADC-TR-87-262 F19628-85-K-0038 F/G 9/1 NL



MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS-1963-A

power. This energy absorption limitation at the onset of melting results in the formation of a molten zone which is highly controllable, with relatively large power changes in the upper strip having an incremental effect on the molten zone morphology. This optical energy absorption limitation provides a texture assumption mechanism for the recrystallized film. This highly controlled energy absorption around the melting point of the polycrystalline film results in a stable coexistence of liquid and solid, with the crystallites of lowest free energy persisting. In the silicon system, crystallites of (100) orientation persist, and form a transition region which seeds the recrystallizing silicon film. Thus, radiatively heated polycrystalline silicon films possess a texture-dependent melting point, with a (100) textured transition region.

Figure C.1 contains an illustration of the formation of a molten zone via the non-coherent, radiative graphite strip. The intensity gradients and the thermal gradients in the lateral direction from the molten zone are also depicted, as they have a significant influence on the liquid-solid interface morphology and agglomeration. In the case of the graphite strip, the intensity gradients and the temperature gradients lateral to the molten zone are not severe, and are generally referred to as the low gradient case. The intensity gradient at the trailing edge of the liquid-solid interface perturbs the liquid-solid interface, and results in an equilibrium interface morphology. The period of the interface structure is a function of the absorptivity of the liquid and the solid and the thermal conductivity of the liquid, solid and the substrate material. The equilibrium shape of the liquid-solid interface is the most prominent influence on the defect structure in the recrystallized films. Cellular and primary dendridic interface morphologies are preferred, as they result in the lowest density of subboundaries in the recrys-

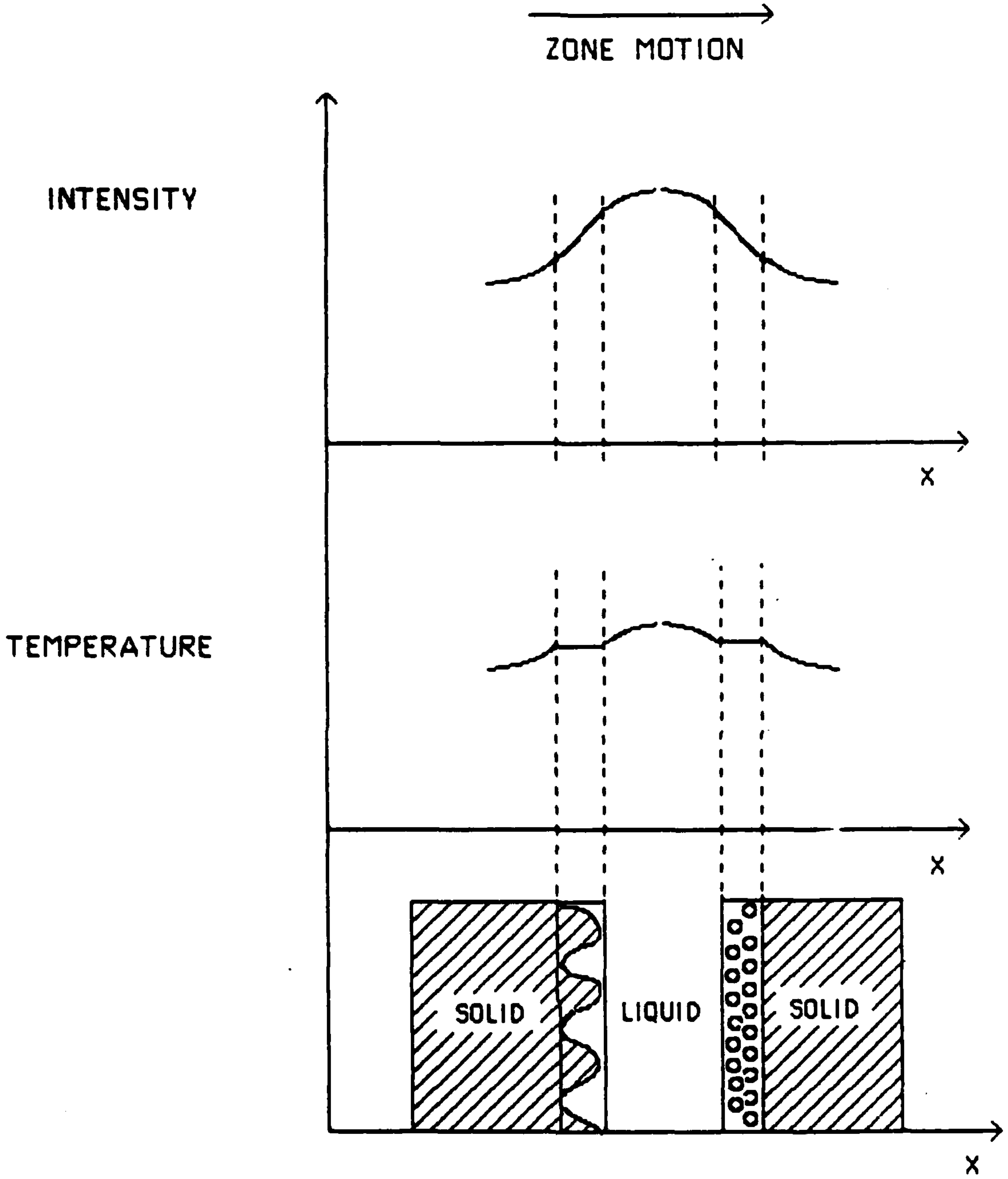


FIGURE C.1 Intensity gradient, thermal gradient, interface morphology for graphite strip primary heating source. The positive X axis is the direction of zone motion.

tallized films. Cellular and primary dendridic interfaces occur in the lowest intensity gradient case.

The low gradient in intensity lateral to the liquid zone also results in a relatively low thermal gradient in this direction. This is desirable, as thermal forces exerted upon the capping structure due to expansion against a rigid restraint are not developed. Hence, cap failure which could result in agglomeration is avoided.

The electron beam primary heating system is characterized by a purely conductive mode of heat transfer to the polysilicon layer. To first order, the energy absorption from an electron beam source is dependent only upon the density and the atomic number of the target (sample) irradiated. There is no significant limitation of energy absorption of the polysilicon upon phase change. Since transition region analogous to the radiative heating scheme is not formed, seeding from (100) crystallites does not occur. The assumed texture mechanism for electron beam heated silicon films is absolute undercooling. The texture of electron beam heated material is generally (111). Figure C.2 contains an illustration of the formation of a molten zone with a focused electron beam. The intensity gradients and thermal gradients in the lateral direction from the molten zone are severe. As indicated, no significant transition region is created.

The high gradient in intensity at the trailing edge of the molten zone result is in the formation of a faceted growth front which is probably bounded by (111) planes. The formation of cellular interfaces is highly improbable, as the region of stable coexistence of liquid and solid at the trailing edge is very narrow. The high gradients in intensity at the trailing edge of the molten zone result in defect structures which are more dense than those of the low gradient case.

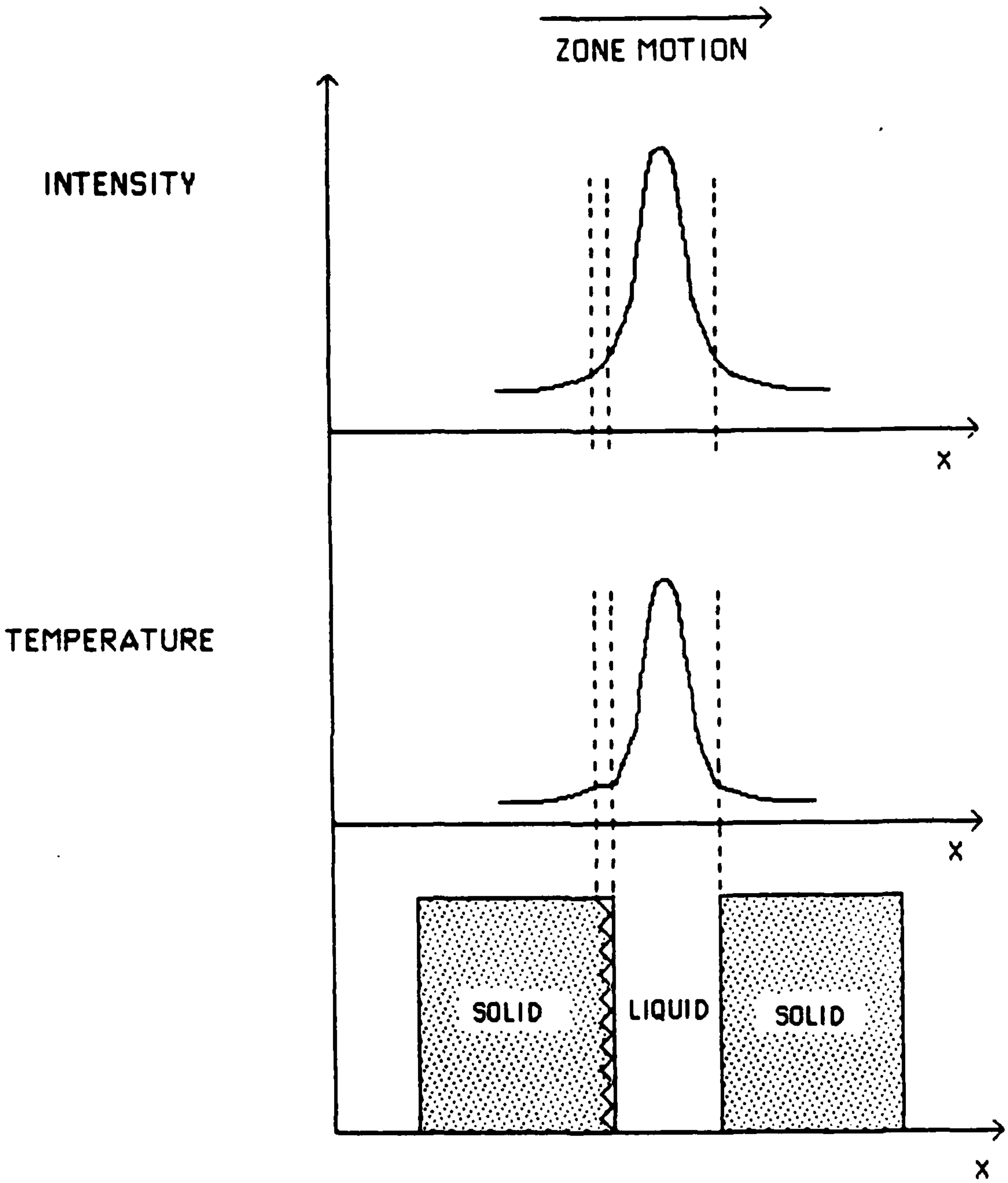


FIGURE C.2 Intensity gradient, thermal gradient, interface morphology for electron beam primary heat source. The positive X axis is the direction of zone motion.

The high intensity gradient at the liquid-solid interface results in extremely high lateral temperature gradients in the capping structure. Upon application of the electron beam, the silicon dioxide cap directly above the molten zone is forced to expand against relatively cold, rigid supports. This results in the development of large thermal forces within the cap with the possibility of inducing mechanical failure.

The most significant advantage of the electron beam is the ability to tailor the energy density within the SOI structure. The spatial peak of energy absorption is a function of beam acceleration voltage and target atomic number and density. It is possible to select beam parameters which result in maximum energy absorption in the polysilicon and hence control the vertical temperature profile within the structure. This also reduces radiation dampage to the capping structure. The ability to focus an electron beam is also a function of acceleration voltage, with narrow molten zone possible at higher beam voltages. Thus, the selection of beam voltage is often a compromise between desired energy absorption and molten zone width.

It is clear that the energy absorption, texture assumption mechanism, and liquid-solid interface morphology are different for the electron beam and the graphite strip primary sources. The relative advantage of the primary heating sources depends upon the particular application. For continuous films, the graphite strip has the advantage due to low defect density within the recrystallized films. However, for patterned films the electron beam may offer key advantages. It was mentioned in Chapter 3 that the stress level in the polysilicon layers may be significantly reduced by utilizing a PSG visoelastic energy absorption sublayer. The time constant for strain relief of a square island is proportional to the linear dimension squared, so small islands may experience significant strain relief prior to the application of the primary source. Hence, it is advantageous to recrystallize small islands (400 µm x 400 µm) on alumina substrates.

Recrystallization of an island structure results in a disturbance of the crystallographic information within the film. Within the graphite strip heater (low gradient) system, the film texture is dependent upon the (100) seeds in the original transition region. When the recrystallization front encounters an isolated polysilicon island, all crystallographic information of the recrystallized film is disturbed. The island will assume a new texture based upon absolute undercooling; hence, (111) texture will be preferred. However, since the intensity gradient at the trailing edge of the molten zone is low, undercooled crystallites will nucleate and propogate a long distance into the molten zone. The resulting morphology will consist of a tangled area of (111) crystallites, and to a large degree the film will be polycrystalline. One way to inhibit this undesired recrystallization process is to reduce the upper strip power and to stop the zone translation in order to re-establish a transition region. This is inherently a small-area process, with many islands being sacrificed.

The electron beam will not suffer such a drastic change in texture upon encountering an isolated island, as the texture is not strongly dependent upon the original seeds. The high gradient at the trailing edge of the molten zone will not permit the (111) crystallites to propogate a significant distance into the molten region. It is highly probable that faceted growth will persist.

Appendix D

Preliminary Pin Diode Microwave Test Results

As mentioned in Section 4.4, microwave test results were obtained using the single-crystal silicon PIN diodes to demonstrate the capability of our process using the mounting scheme described in Section 4.4. Since our technique had been designed based upn the silicon-on-alumina structure, the increased dissipation in the 10-20 ohm-cm Si substrate prevented complete diode characterization. However, excellent conductivity modulation has been demonstrated as described in this section.

The key measurement to determine the microwave performance of novel PIN diodes is that of RF resistance versus forward DC bias current. The measurement setup in our laboratory consists of a 2 to 4 GHz sweep oscillator, a low pass filter, a circulator, two variable attenuators, two 10-dB directional couplers, a crystal detector, two bias tees, and several terminations. The low pass filter is placed at the output of the signal source to block higher harmonics. The circulator is used with a 50 ohm termination as an isolator to reduce the effects of reflections. The directional couplers allow the measurement of incident, reflected and transmitted power.

Once the PIN diode has been mounted in series with the 50 ohm transmission line, its RF resistance can be calculated from data of reflected and transmitted power. However, this requires a uniform transmission structure without significant discontinuities or dissipation. In flip mounting the RF testable devices, both the reflected and transmitted power were approximately

13 dB down from the incident power without any DC bias. As reverse DC bias voltage was applied (to deplete the I-layer), little change in RF characteristics was observed (as expected since the junction capacitance is quite small). As the DC forward bias was increased, more power was transmitted, demonstrating conductivity modulation. However, a limit was reached at 5.5 dB below the incident power. Although the ability to control the amount of transmitted power by varying the bias conditions is evidence that the PIN diode is being conductivity modulated, the loss of most of the incident power was of great concern. In particular, without DC bias most of the incident power should be reflected. Using additional microwave tests, we demonstrated that the 10-20 ohm-cm substrate was the dominant source of this dissipation. That is, there is significant RF dissipation resulting from the flip mounting in the transmission section between the text fixture and the PIN diode.

To obtain some quantification of the degree of conductivity modulation, a device identical to those which had been measured was "shorted" using an indium perform of 1.7 ohms DC resistance. The chip was then flip-mounted as before and the RF measurements repeated. The transmitted power was 6 db below the incident power, indicating that under forward bias, the resistance of the I-region was comparable to that of the indium preform. Thus, we conclude excellent conductivity modulation has been obtained, even though the RF resistance dependence upon DC bias current cannot be obtained. Furthermore, the change in the transmitted RF power commenced at a relatively low forward current of approximately 10 uA, indicating an excellent quality device for 10-20 ohm-cm I-layer resistivity. Referring to the log I versus V plot in Figure 5.3, this current level occurs near the start of the region where the ideality factor is slightly greater than two (0.6 to 0.8V), confirming that this region corresponds directly to double injection and conductivity modulation.

With the combination of these promising RF conductivity modulation results and the high reverse DC breakdown voltage (150V to 200V as reported in Chapter 4), we conclude that the lateral PIN diode structure with doped polysilicon injecting contacts is compatible with high power microwave monolithic control circuits.

END
DATE
FILMED
6-1988
DTIC